DATA SHEET

OM6208
65 x 96 pixels matrix grey-scale LCD driver

Product specification
Supersedes data of 2003 Jan 30

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Philips
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CONTENTS

65 x 96 pixels matrix grey-scale LCD driver OM6208

1 FEATURES

- Single chip LCD Multiple Row Addressing (MRA) grey-scale/colour controller/driver
- Four grey levels/colours
- 65 row outputs and 96 column outputs
- Display Data RAM (DDRAM) $65 \times 96 \times 2$ bits
- Selectable interface:
  - 6.5 MHz 3-line or 4-line Serial Peripheral Interface (SPI)
  - 6.5 MHz 3-line serial interface
  - High speed I^2C-bus interface.
- On-chip:
  - Configurable voltage multiplier generating V_{LCD}; external V_{LCD} also possible
  - Four-segment V_{LCD} temperature compensation
  - Generation of intermediate LCD bias voltage
  - Oscillator requires no external components; external clock input also possible
  - Integrated charge pump capacitors (reducing total system cost).
- External reset input
- Temperature read-back
- Selectable N-line inversion and frame inversion
- CMOS compatible inputs
- Logic supply voltage range 1.7 to 3.3 V
- High-voltage generator supply voltage range 2.4 to 4.5 V
- Display supply voltage range 5 to 9 V
- Low power consumption; suitable for battery operated systems
- Programmable row pad mirroring for compatibility with Tape Carrier Packages (TCP) and with Chip-On Glass (COG) applications
- Status read which allows chip recognition
- Start address line; for example, for scrolling the displayed image
- Slim chip layout; suitable for COG, COF and TCP applications
- Operating temperature range –40 to +85 °C.

2 APPLICATIONS

- Telecom equipment
- Portable instruments
- Point of sale terminals.

3 GENERAL DESCRIPTION

The OM6208 is a low power CMOS LCD controller driver, designed to drive a graphic display of 65 rows and 96 columns. All necessary functions for the display are provided in a single chip, including on-chip generation of LCD supply and bias voltages, resulting in a minimum of external components and low power consumption. The OM6208 can be interfaced to microcontrollers via a serial bus and I^2C-bus.

The OM6208 is manufactured in n-well CMOS technology.

Operation is with the substrate at V_{SS} potential.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
OM6208MU/2DA/1	–	chip with bumps in tray	–

5 BLOCK DIAGRAM

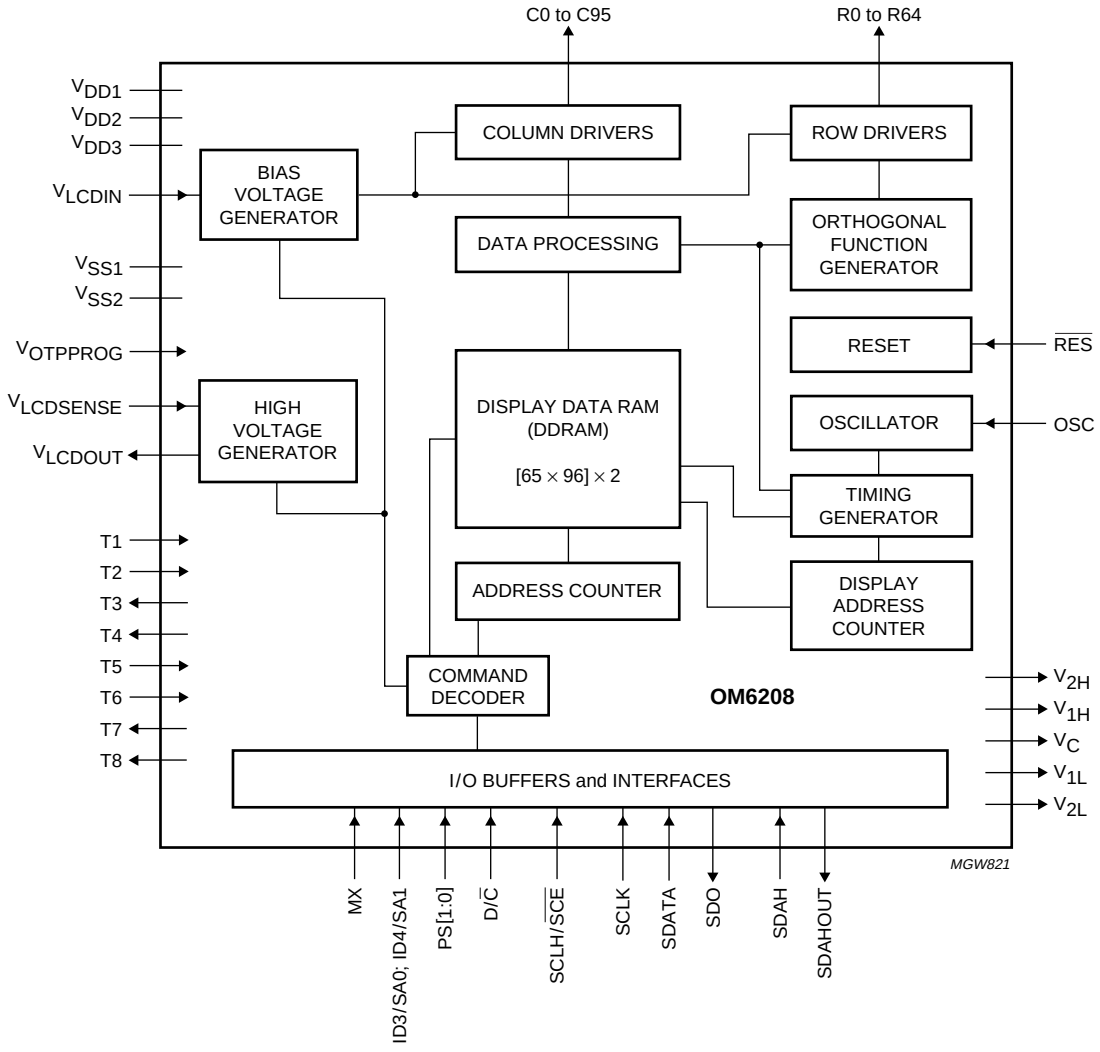


Fig.1 Block diagram.

6 PINNING

SYMBOL	PAD[1]	DESCRIPTION
V_{LCDIN}	5 to 8	LCD supply voltage input; note 2
V_{LCDOUT}	9 to 15	LCD supply voltage output from high voltage generator; note 2
$V_{LCDSENSE}$	16	regulation input to high voltage generator; note 2
V_{DD2}	17 to 26	supply voltage 2; note 3
V_{DD3}	27 to 29	supply voltage 3; note 3
OSC	30	oscillator input; note 4
D/$\overline{C}$	31	data/$\overline{\text{command}}$ input/output; note 5
PS[1:0]	32 and 33	interface selection inputs
V_{DD1}	34 to 39	supply voltage 1; note 3
SDAHOUT	44	I^2C-bus data output; note 6
SCLK	46	serial data clock input; used in 3-line or 4-line SPI or 3-line serial interface mode
SDAH	52	I^2C-bus data input; note 7
SDO	53	serial data output; note 8
SDATA	54	serial data input; note 9
V_{SS2}	55 to 61	ground 2 (analog ground); note 10
V_{SS1}	62 to 67	ground 1 (digital ground); note 10
MX	68	horizontal mirroring input
T3	69	test outputs; note 11
T4	70	
T1	71	
T2	72	
T5	73	
T6	74	
ID3/SA0; ID4/SA1	75 and 76	manufacturer device identification/I^2C-bus slave address input pads; note 12
V_{DD1}	77	supply voltage 1 (tie-off pad)
SCLH/$\overline{\text{SCE}}$	83	I^2C-bus clock input/serial chip enable input in 3-line or 4-line SPI mode; note 5
$V_{OTPPROG}$	84 to 86	supply voltage input for OTP programming; note 13
$\overline{\text{RES}}$	88	external reset input; active low; must be applied to initialize the chip properly
R32 to R64	105 to 137	LCD row driver outputs
V_C	138	bias buffer output; note 14
T8	141	test outputs; note 11
T7	142	
V_{1L}	143	bias buffer output; note 14
C95 to C48	144 to 191	LCD column driver outputs
C47 to C0	194 to 241	
R31 to R0	247 to 278	LCD row driver outputs
V_{1H}	244	bias buffer outputs; note 14
V_{2L}	245	
V_{2H}	246	

Notes

1. Dummy pads are located at positions 1, 2, 4, 40 to 43, 45, 47 to 51, 78 to 82, 87, 89 to 92, 95 to 104, 139, 140, 192, 193, 242, 243, 279 and 280; alignment marks are located at positions 3 and 93; an alignment bump is located at position 94.
2. Positive power supply for the liquid crystal display (see also Figs 38, 39 and 40):
   a) If the internal voltage generator is used, pads V_{LCDIN}, $V_{LCDSENSE}$ and V_{LCDOUT} must be connected together.
   b) An external LCD supply voltage can be incorporated using the V_{LCDIN} pad; the internal voltage generator must then switched off, pad V_{LCDOUT} must be open-circuit (not connected to pad V_{LCDIN}) and pad $V_{LCDSENSE}$ connected to the V_{LCDIN} input; $V_{DD2,3}$ should be applied according to the specified voltage range. In Power-down mode, the external LCD supply voltage must be switched off.
3. V_{DD2} and V_{DD3} supply the internal voltage generator, both have the same voltage and may be connected together outside of the chip; V_{DD1} supplies the remainder of the chip. V_{DD1}, V_{DD2} and V_{DD3} can be connected together but then care must be taken with respect to the supply voltage range.
4. When the on-chip oscillator is used, the OSC input must be connected to V_{DD1}. If an external clock signal is used, then this is connected to the OSC input. If both the oscillator and external clock are inhibited by connecting pad OSC to V_{SS1}, the display is not clocked and may be in a DC state. To avoid this, the chip should always be put into Power-down mode before stopping the clock.
5. This input is not used with the 3-line serial interface and must be connected to V_{DD1} or V_{SS1} when this interface is in use.
6. SDAHOUT is the serial data acknowledge output from the I^2C-bus interface. By connecting SDAHOUT to SDAH externally, the SDAH line becomes fully I^2C-bus compatible. Having the acknowledge output separated from the serial data line is advantageous in COG applications because here the track resistance from the SDAHOUT pad to the system SDAH line can be significant and a potential divider can be generated by the bus pull-up resistor and the ITO track resistance. It is possible that during the acknowledge cycle the OM6208 will not be able to create a valid logic 0. By splitting the SDAH input from the SDAHOUT output the device could be used in a mode that ignores the acknowledge bit. Therefore in COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAHOUT pad to the system SDAH line to guarantee a valid logic 0. When SDAHOUT is not used, it must be connected to V_{DD1} or V_{SS1}.
7. When I^2C-bus is not used, this pad must be connected to V_{DD1} or V_{SS1}.
8. SDO is a push-pull output; when it is intended to use the readback function of the OM6208, this pad must be connected to the SDATA pad, or used separately; when I^2C-bus interface is selected, this pad should be connected to V_{DD1} or V_{SS1}.
9. When I^2C-bus interface is selected this pin should be connected to V_{DD1} or V_{SS1}.
10. Supply rails V_{SS1} and V_{SS2} must be connected together.
11. Test pads T1 to T8 are not accessible to users: T1, T2, T5 and T6 must be connected to V_{SS}; T3, T4, T7 and T8 must be open-circuit.
12. Module identification bits: these bits may be read back via the ‘read back’ instruction; when the I^2C-bus interface is being used, these bits are the two LSBs of the slave address.
13. V_{OTPROG} can be connected to SCLH/$\overline{SCE}$ pad to reduce the external connections. If not connected in this configuration, then V_{OTPROG} should be open-circuit during normal operation.
14. These pads are not accessible to users and must be left open-circuit; an explanation of the bias buffer function is given in Section 11.9.

7 FUNCTIONAL DESCRIPTION

7.1 I/O buffers and interfaces

One of four industrial standard interfaces can be selected using the interface configuration inputs PS1 and PS0.

Table 1 Serial/I^2C-bus interface selection

PS1	PS0	SELECTED INTERFACE
0	0	3-line SPI
0	1	4-line SPI
1	0	I^2C-bus interface
1	1	3-line serial interface

7.2 Oscillator

The on-chip oscillator provides the clock signal for the display system. No external components are required when the internal oscillator is used. An external clock signal, if used, is connected to this input.

7.3 Address counter

The Address Counter (AC) assigns addresses to the display data RAM for writing. The X address X[6:0] and the Y address Y[4:0] are set separately.

7.4 Display data RAM

The OM6208 contains a $65 \times 96 \times 2$ bit static RAM which stores the display data. The display data RAM is divided into 17 banks of 96 bytes, although only two bits of the 17th bank are used. During RAM access, data is transferred to the RAM via the serial interface. There is a direct correspondence between X address and column output number.

7.5 Display address counter

The display is generated by simultaneously reading out the RAM content for two or four rows, depending on the current display size that is selected. This content will be processed with the corresponding set of two or four orthogonal functions and so generate the signals for switching the pixels of the display on or off according to the RAM content.

The display status (all dots on/all dots off and normal/inverse video) is set by the bits DON, DAL and E in the command Display control (see Table 8).

7.6 Timing generator

The timing generator produces the various signals required to drive the internal circuitry. Internal chip operation is not affected by operations on the data bus.

7.7 Data processing

The data processing block receives data from the RAM and the orthogonal function from the logic circuits, then selects the correct voltage level to be provided to the columns.

7.8 High voltage generator

The high voltage generator provides the programmed V_{LCD} to the bias voltage generator block.

7.9 Bias voltage generator

The bias voltage generator generates all the voltage levels required for the MRA driving system.

7.10 Command decoder

The command decoder identifies command words arriving at the interface and routes the data bytes that follow to their destination.

7.11 Orthogonal function generator

The orthogonal function generator generates a set of orthogonal functions suitable for the selected value of p (number of active rows).

7.12 Reset

The reset block handles the hardware reset input ($\overline{RES}$) and software reset and provides all internal blocks with the required reset signal.

7.13 Row drivers and column drivers

The OM6208 contains 65 row and 96 column drivers which connect the appropriate LCD bias voltages in sequence to the display in accordance with the data to be displayed. A typical MRA driving scheme with waveforms for p = 4 is shown in Fig.2. The value of p represents the number of simultaneously selected rows.

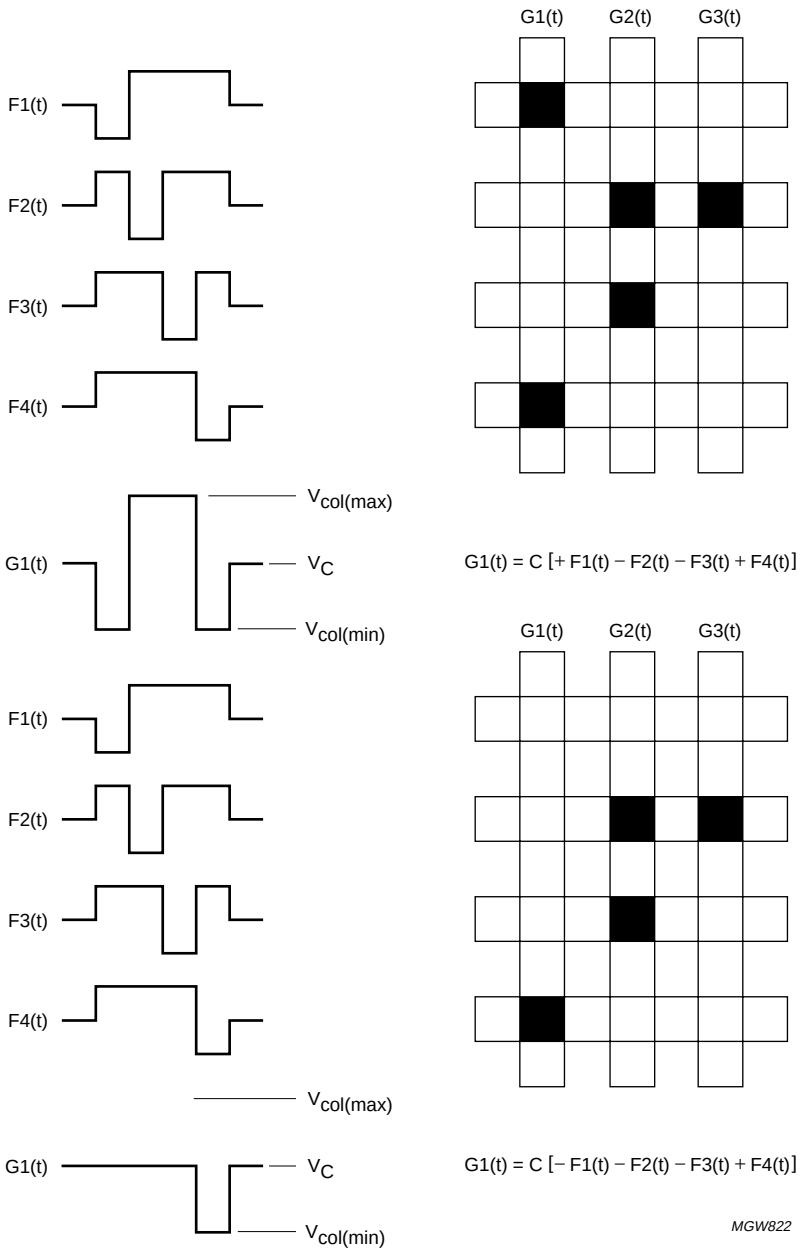


Fig.2 Typical MRA LCD driver waveforms for p = 4.

8 RAM ADDRESSING

Data is downloaded in bytes into the RAM matrix of the OM6208 as indicated in Fig.3. The display RAM has a matrix of 65 × 96 × 2 bits. The columns are addressed by the address pointer. The address ranges (decimal values) are X = 0 to 95 and Y = 0 to 16. The Y address represents the bank number. Addresses outside these ranges are not allowed.

The Data Order Bit (DOR) defines the bit order (LSB on top or MSB on top) for writing into the RAM.

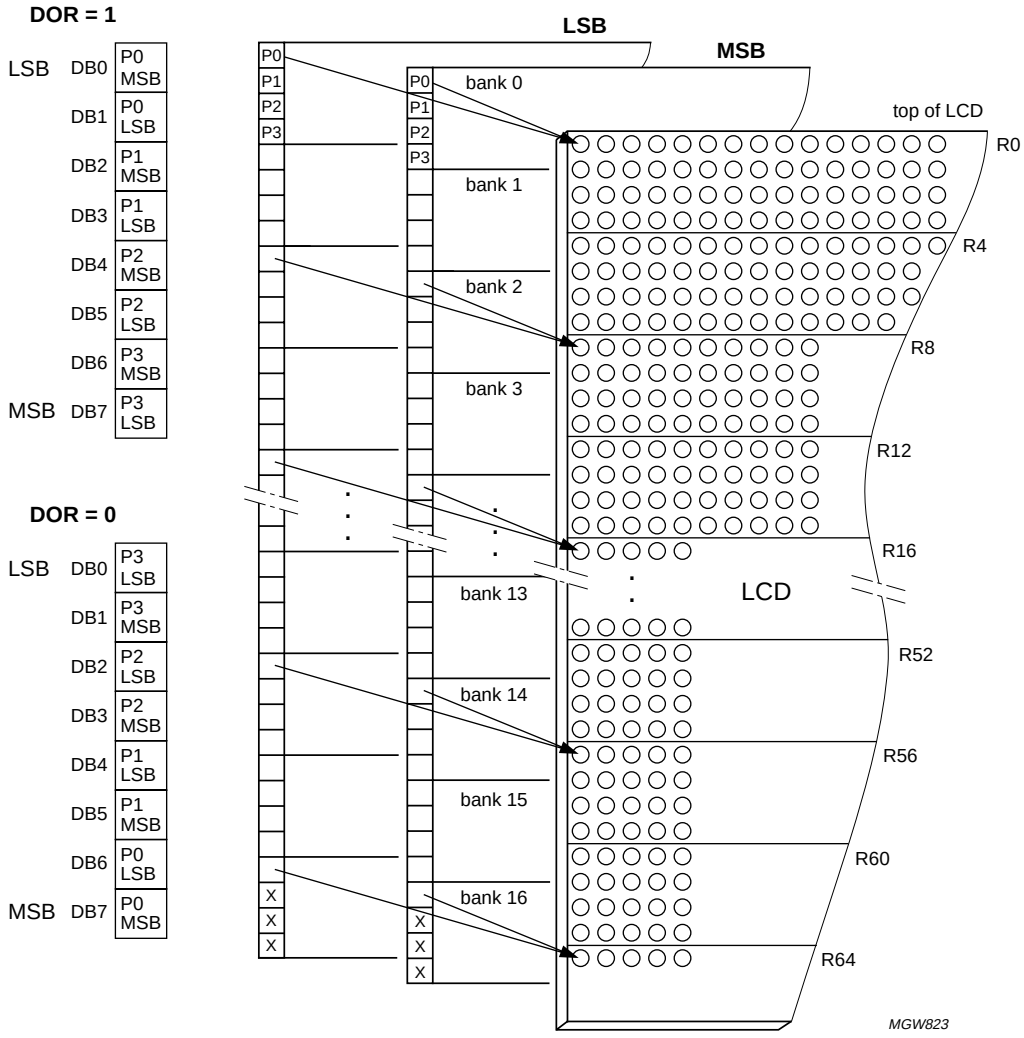


Fig.3 DDRAM-to-display mapping.

8.1 Display data RAM structure

The mode for storing data in the display data RAM is dependent on:

- Horizontal/vertical addressing mode set by bit V in the ‘RAM addressing mode’ instruction
- Data order set by bit DOR in the ‘data order’ instruction
- Mirror the X-axis set by input MX.

8.1.1 HORIZONTAL/VERTICAL ADDRESSING

Two different addressing modes are possible; horizontal addressing mode and vertical addressing mode.

In the horizontal addressing mode (V = 0) the X address increments after each byte. After the last X address (X = 95), X wraps around to 0 and Y increments to address the next row (see Fig.4).

In the vertical addressing mode (V = 1), the Y address increments after each byte. After the last Y address (Y = 16), Y wraps around to 0 and X increments to address the next column (see Fig.5).

After the very last address, the address pointers wrap around to address X = 0 and Y = 0 in both horizontal and vertical addressing modes.

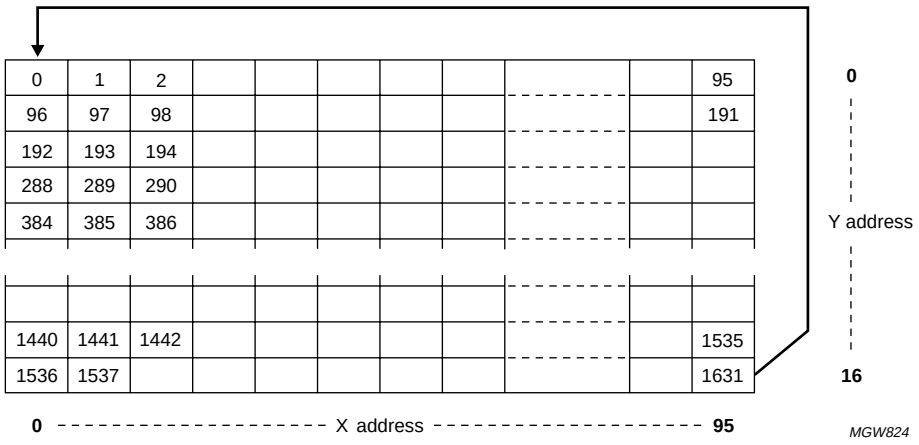


Fig.4 Sequence of writing data bytes into RAM with horizontal addressing (V = 0).

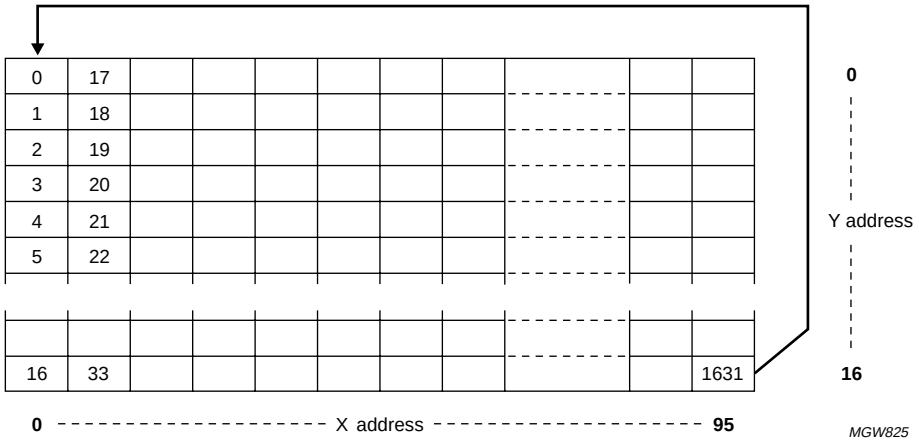


Fig.5 Sequence of writing data bytes into the RAM with vertical addressing (V = 1).

8.1.2 MIRROR Y

The Mirror Y (MY) bit allows vertical mirroring:

- When MY = 1, the Y address space is mirrored; the address Y = 0 is then located at the bottom of the display (see Fig.6)
- When MY = 0, the mirroring is disabled and the address Y = 0 is located at top of the display (see Fig.7).

Refer also to Section 11.6.

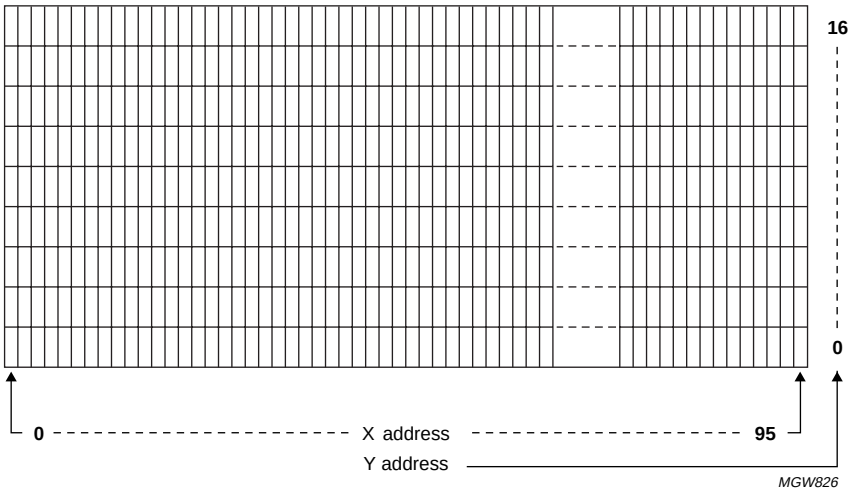


Fig.6 RAM format addressing (MY = 1).

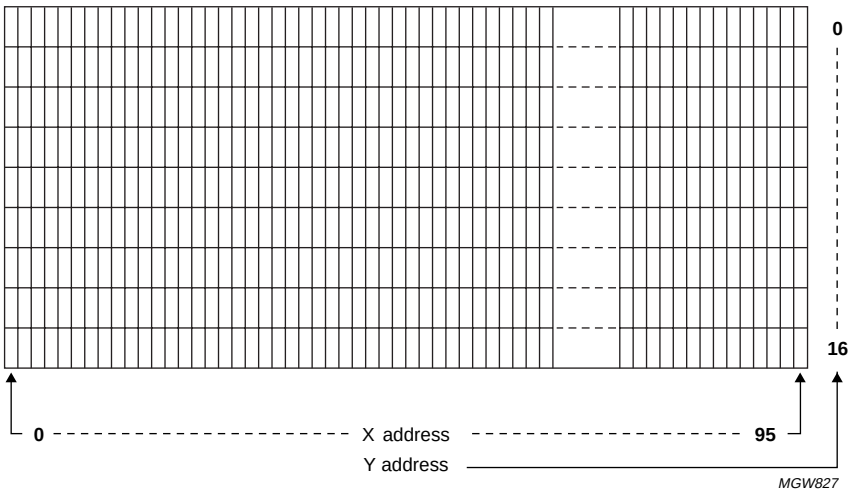


Fig.7 RAM format addressing (MY = 0).

8.1.3 MIRROR X

The Mirror X (MX) input allows a horizontal mirroring:

- When MX = 1, the X address space is mirrored; the address X = 0 is then located at the right side (X_{max}) of the display (see Fig.8)
- When MX = 0, the mirroring is disabled and the address X = 0 is located at the left side (column 0) of the display (see Fig.9).

Refer also to Section 11.6.

Fig.8 RAM format addressing (MX = 1).

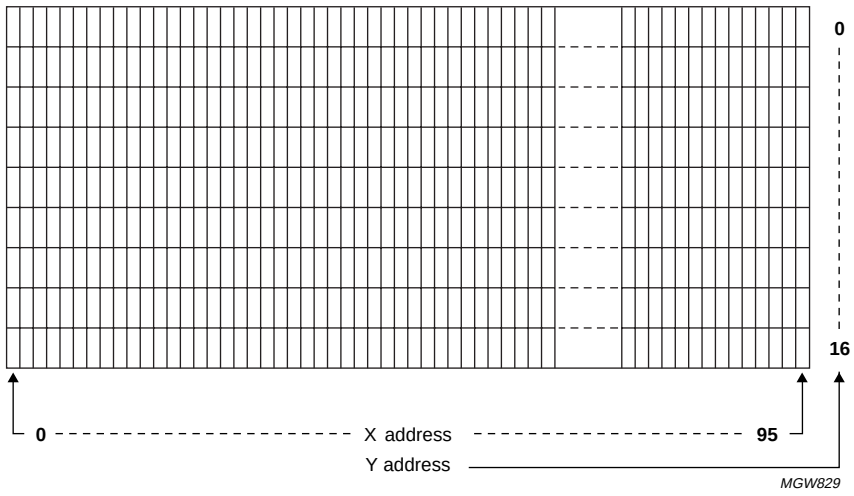


Fig.9 RAM format addressing (MX = 0).

9 SERIAL INTERFACING

Communication with the microcontroller can occur via a clock-synchronized serial peripheral interface. It is possible to select two different 3-line (SPI and serial interface) or a 4-line SPI interface. Selection is done via the PS[1:0] inputs.

9.1 Serial peripheral interface

The Serial Peripheral Interface (SPI) is a 3-line or 4-line interface for communication between the microcontroller and the LCD driver chip. Three lines are common to both 3-line and 4-line SPI, these are $\overline{SCE}$ (chip enable), SCLK (serial clock) and SDATA (serial data). For the 4-line SPI a separate D/$\overline{C}$ line is added. The OM6208 is connected to the serial data I/O of the microcontroller by pads SDATA (data input) and SDO (data output) connected together.

9.1.1 WRITE MODE

The display data/command indication may be controlled by software or by the D/$\overline{C}$ select pin. When the D/$\overline{C}$ pad is used, display data is transmitted when D/$\overline{C}$ is HIGH, and command data is transmitted when D/$\overline{C}$ is LOW (see Figs 10 and 11). When D/$\overline{C}$ is not used, the 'display data length' instruction is used to indicate that a specific number of display data bytes (1 to 255) are to be transmitted (see Fig.11). The next byte after the display data string is handled as an instruction command.

When the 3-line SPI interface is used the display data/command is controlled by software (see Fig.12).

If $\overline{SCE}$ is pulled high during a serial display data stream, the interrupted byte is invalid data but all previously transmitted data is valid. The next byte received will be handled as an instruction command (see Fig.13).

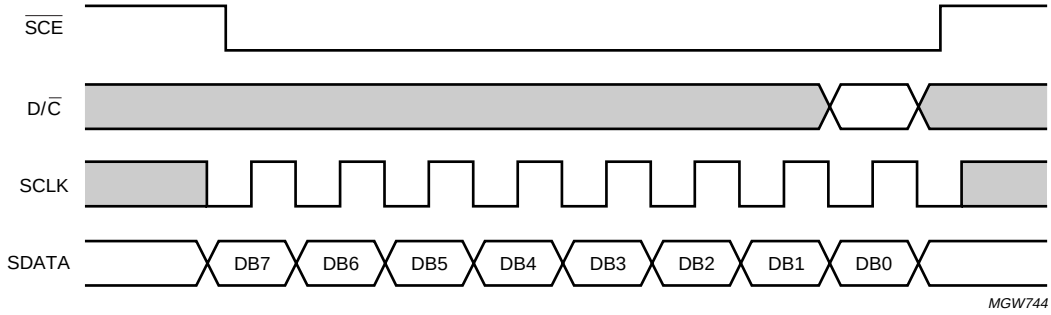


Fig.10 4-line SPI bus protocol; transmission of one byte.

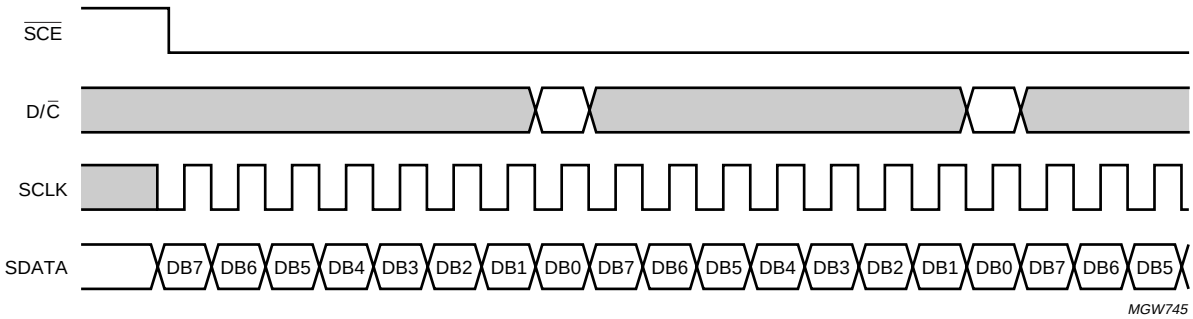


Fig.11 4-line SPI bus protocol; transmission of several bytes.

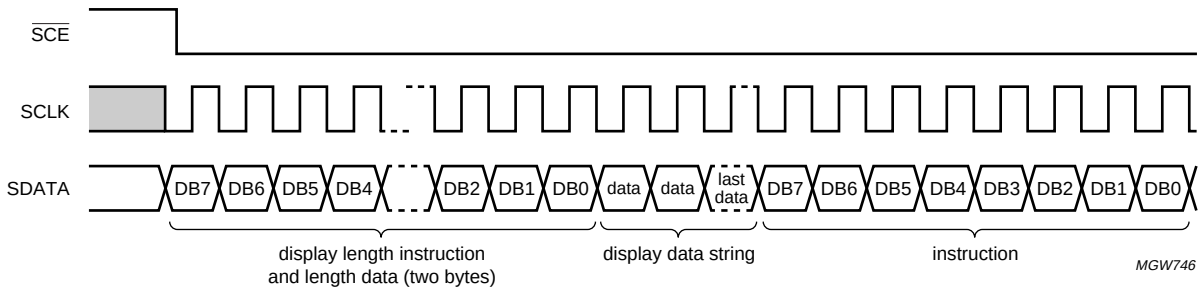


Fig.12 3-line SPI bus protocol; transmission of several bytes.

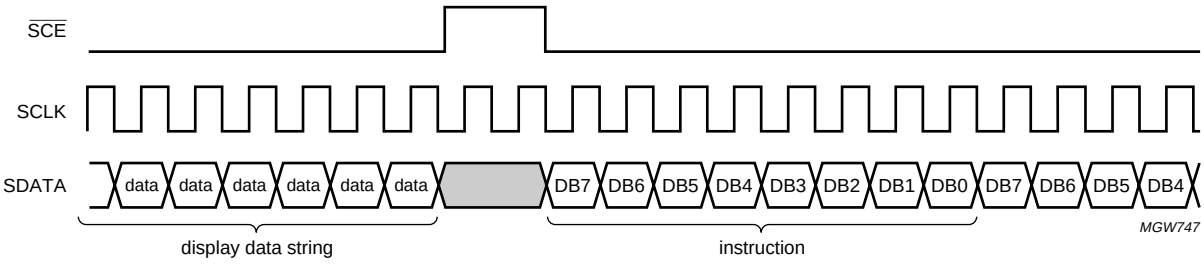


Fig.13 3-line SPI bus protocol: transmission interrupted by $\overline{SCE}$.

9.1.2 READ MODE

The read mode of the interface means that the microcontroller reads data from the OM6208. To do so the microcontroller first has to send a command, the read status command, and then OM6208 will respond by transmitting data on the SDO line. After that, $\overline{SCE}$ is required to go HIGH (see Fig.14).

The OM6208 samples the SDATA data at rising SCLK edges, but shifts SDO data at falling SCLK edges. Thus the SDO data is available to be read by the microcontroller at rising SCLK edges.

After the read status command has been sent, the SDATA line must be set to 3-state (high-impedance) not later than at the falling SCLK edge of the last bit (see Fig.14).

For the read data format, see Section 9.2.3; the serial interface timing diagram is given in Chapter 15.

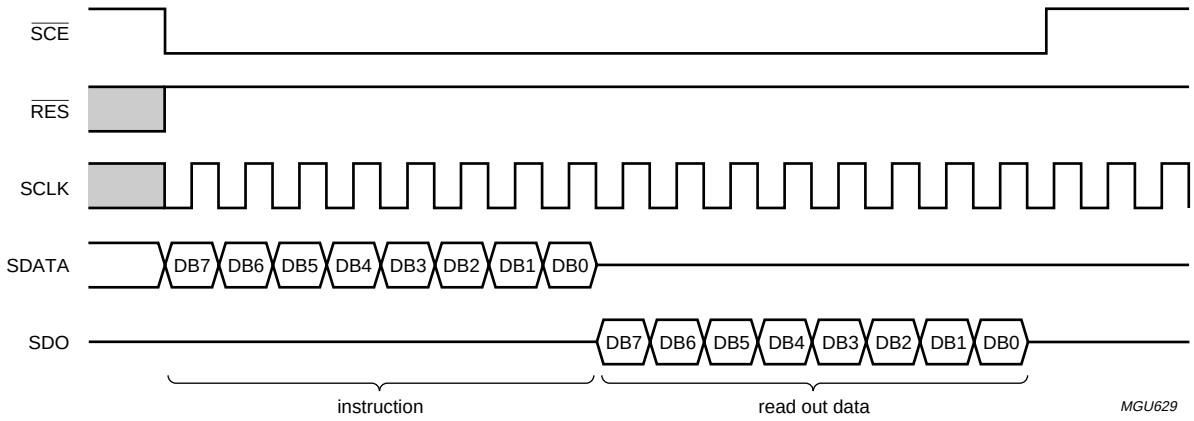


Fig.14 Read mode SPI 3- and 4-line interfaces.

9.2 Serial interface (3-line)

The serial interface is also a 3-line bidirectional interface for communication between the microcontroller and the LCD driver chip. The three lines are $\overline{SCE}$ (chip enable), SCLK (serial clock) and SDATA (serial data). The OM6208 is connected to the SDA of the microcontroller by the SDATA (data input) and SDO (data output) pads which are connected together.

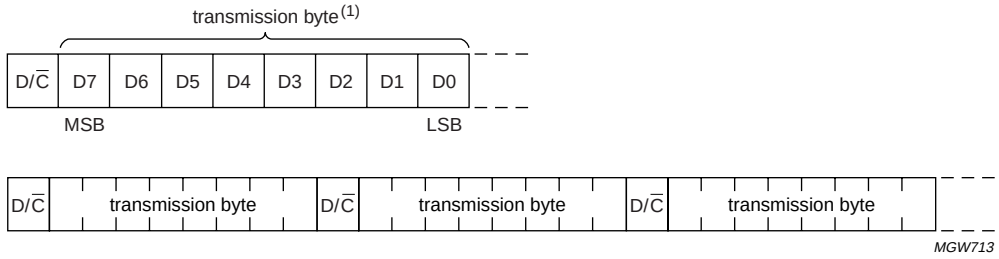
9.2.1 WRITE MODE

The write mode of the interface means that the microcontroller writes instructions and data to the OM6208. Each data packet contains a control bit D/$\overline{C}$ and a transmission byte. If D/$\overline{C}$ is LOW, the following byte is interpreted as command byte. The instruction set is given in Table 7. If D/$\overline{C}$ is HIGH, the following byte is stored in the display data RAM. After every data byte the address counter is incremented automatically. The general format of the write mode and the definition of the transmission byte is shown in Fig.15.

Any instruction can be sent in any order to the OM6208. The MSB is transmitted first. The serial interface is initialized when $\overline{SCE}$ is HIGH. In this state, SCLK clock pulses have no effect and no power is consumed by the serial interface. A falling edge on $\overline{SCE}$ enables the serial interface and indicates the start of data transmission.

Figures 16, 17 and 18 show the protocol of the write mode:

- When $\overline{SCE}$ is HIGH, SCLK clocks are ignored. During the HIGH time of $\overline{SCE}$ the serial interface is initialized (see Fig.16)
- At the falling $\overline{SCE}$ edge, SCLK must be LOW (see Fig.32)
- SDATA is sampled at the rising edge of SCLK
- D/$\overline{C}$ indicates whether the byte is a command (D/$\overline{C}$ = 0) or RAM data (D/$\overline{C}$ = 1) byte; it is sampled with the first rising SCLK edge
- If $\overline{SCE}$ stays LOW after the last bit of a command/data byte, the serial interface is ready for the D/$\overline{C}$ bit of the next byte at the next rising edge of SCLK (see Fig.17)
- A reset pulse with $\overline{RES}$ interrupts the transmission. The data being written into the RAM may be corrupted. The registers are cleared. If $\overline{SCE}$ is LOW after the rising edge of $\overline{RES}$, the serial interface is ready to receive the D/$\overline{C}$ bit of a command/data byte (see Fig.18).



(1) A transmission byte may be a command byte or a data byte.

Fig.15 Serial data stream, write mode.

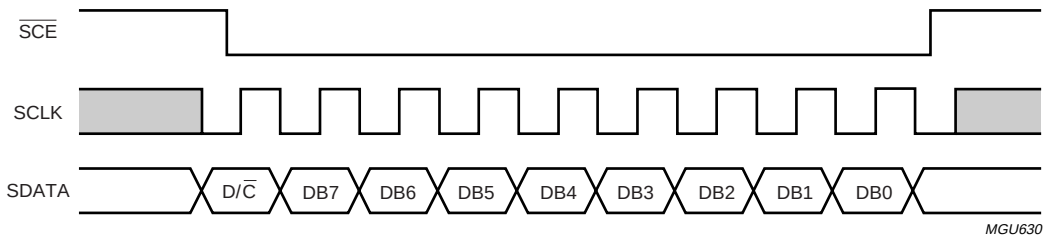


Fig.16 Write mode: a control bit followed by a transmission byte.

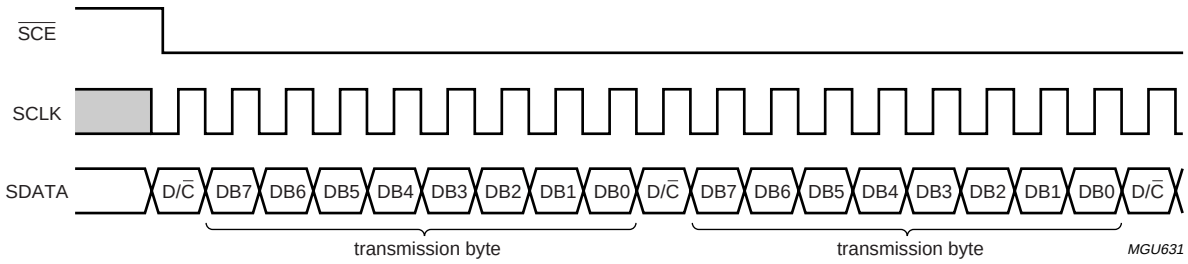


Fig.17 Write mode: transmission of several bytes.

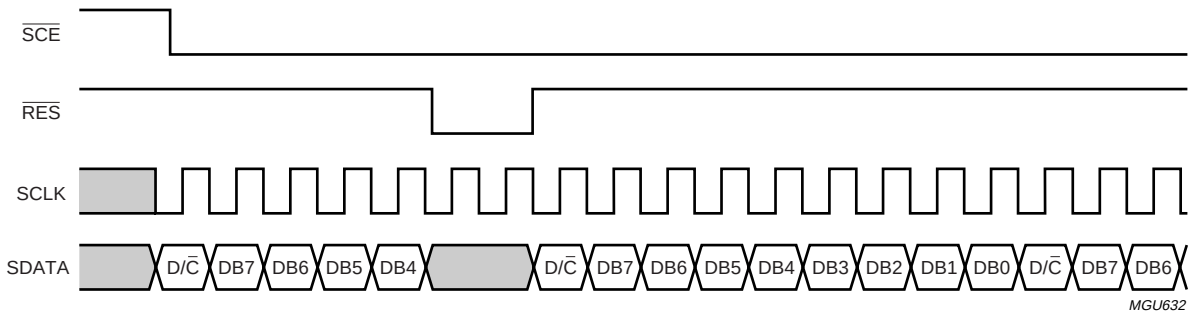


Fig.18 Write mode: interrupted by reset ($\overline{RES}$).

9.2.2 READ MODE

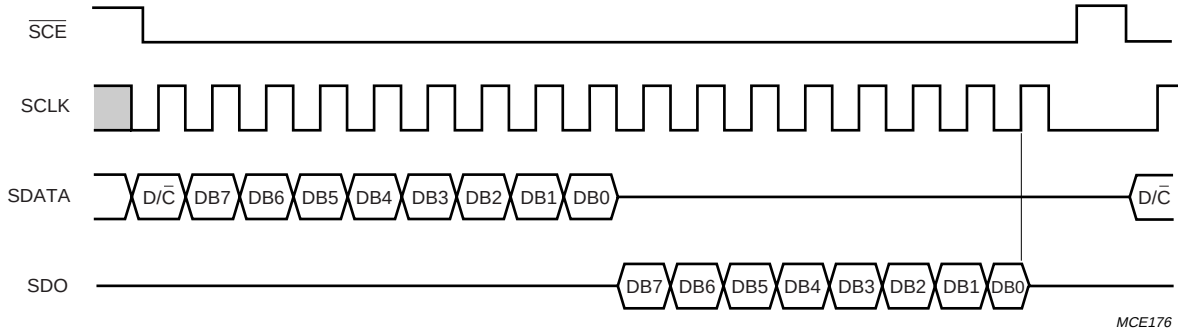


Fig.19 Read mode serial interface 3-line.

The read mode of the interface means that the microcontroller reads data from the OM6208. To do so the microcontroller first has to send a command, the read status command, and then the following byte is transmitted in the opposite direction using SDO (see Fig.19). After that, $\overline{SCE}$ is required to go HIGH before a new command is sent.

The OM6208 samples the SDATA data at rising SCLK edges and shifts SDO data at falling SCLK edges. Thus the SDO data is available for the microcontroller to read at rising SCLK edges.

After the read status command has been sent, the SDATA line must be set to 3-state not later then at the falling SCLK edge of the last bit (see Fig.19).

The 8th read bit is shorter than the others because it is terminated by the rising SCLK edge (see Fig.35). The last rising SCLK edge sets SDO to 3-state after the delay time t_4.

9.2.3 READ DATA FORMAT

Regardless of which serial interface is used there are five bits that can be read (ID1 to ID4 and VM) and one temperature register. For the bits, one bit is transmitted per byte read and is selected by issuing the appropriate read instruction from the instruction set. Bits ID1 and ID2 are hard-wired so that ID1 always returns a logic 0 and ID2 always returns a logic 1. Bits ID3 and ID4 are the identification bits and are set via ID3/SA0 and ID4/SA1 pads. The format for the read bit, B, is shown in Table 2.

Table 2 Read data format

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
x[1]	B	B	B	$\overline{B}$	$\overline{B}$	$\overline{B}$	$\overline{B}$

Note

1. x = undefined.

Table 3 Read temperature sensor

Sending the instruction to read back the temperature sensor data will select the following status byte.

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
x[1]	TD[6]	TD[5]	TD[4]	TD[3]	TD[2]	TD[1]	TD[0]

Note

1. x = undefined.

10 I²C-BUS INTERFACE

10.1 Characteristics of the I²C-bus (Hs-mode)

The I²C-bus Hs-mode is for bidirectional, two-line communication between different ICs or modules with speeds up to 3.4 MHz. The only difference between Hs-mode slave devices and F/S-mode slave devices is the speed at which they operate, therefore the buffers on the SDAH output have an open drain. This is the same for I²C-bus master devices which have an open-drain SDAH output and a combination of an open-drain pull-down and current source pull-up circuits on the SCLH output. Only the current source of one master is enabled at any one time and only during Hs-mode. Both lines must be connected to a positive supply via a pull-up resistor.

Data transfer may be initiated only when the bus is not busy.

10.1.1 System configuration

Definition (see Fig.20):

- Transmitter: the device that sends the data to the bus
- Receiver: the device that receives the data from the bus
- Master: the device that initiates a transfer, generates clock signals and terminates a transfer
- Slave: the device addressed by a master
- Multi-master: more than one master can attempt to control the bus at the same time without corrupting the message
- Arbitration: procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted
- Synchronisation: procedure to synchronize the clock signals of two or more devices.

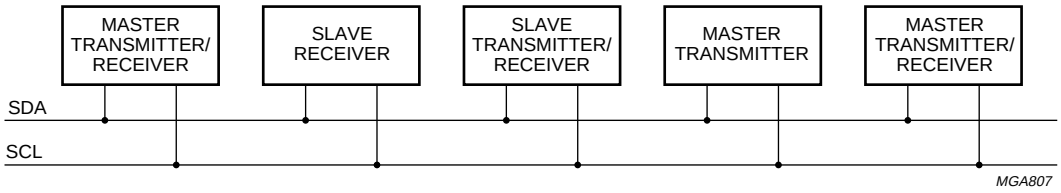


Fig.20 System configuration.

10.1.2 Bit transfer

One data bit is transferred during each clock pulse (see Fig.21). The data on the SDAH line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal.

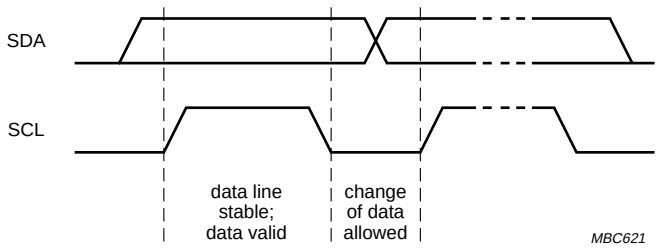


Fig.21 Bit transfer.

10.1.3 START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy (see Fig.22). A HIGH-to-LOW transition of the data line, while the clock is HIGH is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH is defined as the STOP condition (P).

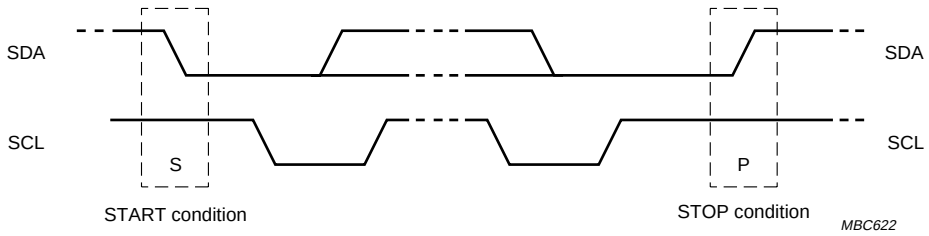


Fig.22 Definition of START and STOP conditions.

10.1.4 ACKNOWLEDGE

Each byte of 8 bits is followed by an acknowledge bit (see Fig.23). The acknowledge bit is a HIGH signal put on the bus by the transmitter during which time the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

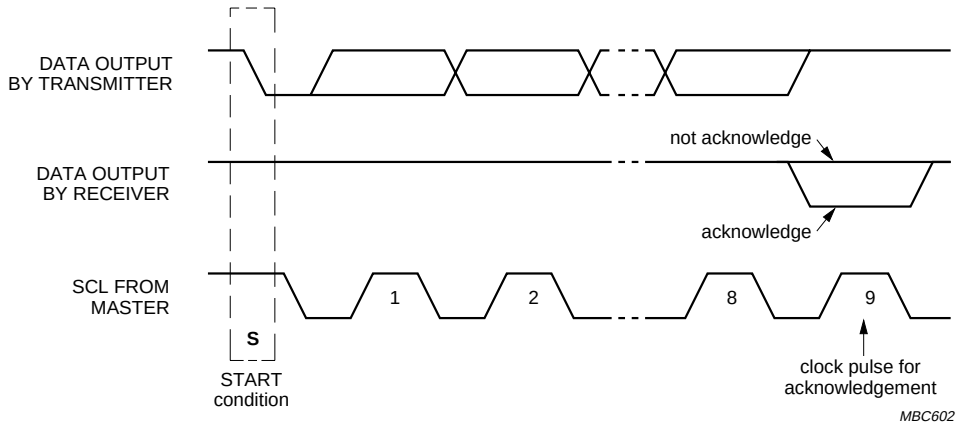


Fig.23 Acknowledge on the I^2C-bus.

10.2 I²C-bus Hs-mode protocol

The OM6208 is a slave receiver/transmitter. If data is to be read from the device the SDAHOUT and SDAH pads must be connected for acknowledge to be used (see Table 1, note 6).

Hs-mode can only commence after the following conditions.

- START condition (S)
- 8-bit master code (00001XXX)
- not-acknowledge bit ($\overline{A}$).

The master code has two functions as shown in Figs 24 and 25, it allows arbitration and synchronization between competing masters at F/S-mode speeds, resulting in one winner. Also the master code indicates the beginning of an Hs-mode transfer.

As no device is allowed to acknowledge the master code, then a master code transmission must be followed by a not-acknowledge ($\overline{A}$). After this $\overline{A}$ bit, and the SCLH line has been pulled up to a HIGH level, the active master switches to Hs-mode and enables at t_H the current-source pull-up circuit for the SCLH signal (see Fig.25).

The active master will then send a repeated START condition (Sr) followed by a 7-bit slave address with a R/$\overline{W}$ bit, and receives an acknowledge bit (A) from the selected slave. After each acknowledge bit (A) or not-acknowledge bit ($\overline{A}$) the active master disables its current-source pull-up circuit. The active master re-enables its current source again when all devices have released and the SCLH signal reaches a HIGH level. The rising of the SCLH is done by a resistor pull-up and so is slower, the last part of the SCLH rise time is speeded up because the current source is enabled. Data transfer only switches back to F/S-mode after a STOP (P) condition.

The write sequence that occurs after the Hs-mode is selected is shown in Fig.26. The sequence is initiated with a START (S) condition from the I²C-bus master which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer.

After an acknowledgement cycle of a write ($\overline{W}$), one or more command words follow which define the status of the addressed slaves. A command word consists of a control byte, which defines Co and D/$\overline{C}$, plus a data byte (see Fig.26 and Table 4).

The last control byte is tagged with a cleared most significant bit, the continuation bit Co. The control and data bytes are also acknowledged by all addressed slaves on the bus.

Table 4 Co and Sr definition

Co	D/$\overline{C}$	R/W	ACTION
0	–	–	last control byte to be sent; only a stream of data bytes are allowed to follow; this stream may only be terminated by a STOP or repeated START condition
1	–	–	another control byte will follow the data byte unless a STOP or repeated START condition is received
–	0	0	data byte will be decoded and used to set up the device
		1	data byte will return the status byte
–	1	0	data byte will be stored in the display RAM
		1	RAM read back is not supported

After the last control byte, depending on the D/$\overline{C}$ bit setting, a series of display data bytes or command data bytes may follow. If the Sr bit was set to logic 1, these display bytes are stored in the display RAM at the address specified by the data pointer. The data pointer is automatically updated and the data is directed to the intended OM6208 device. If the Sr bit of the last control byte was set to logic 0, these command bytes will be decoded and the setting of the device will be changed according to the received commands. The acknowledgement after each byte is made only by the addressed OM6208. At the end of the transmission the I²C-bus master issues a STOP condition (P) and switches back to F/S-mode, however, to reduce the overhead of the master code, it i s possible that a master links a number of Hs-mode transfers, separated by repeated START conditions (Sr).

A read sequence (see Fig.27) follows after the Hs-mode is selected. The OM6208 will immediately start to output the requested data until a not acknowledge is transmitted by the master. The write access should be terminated by a repeated START condition so that the Hs-mode is not disabled.

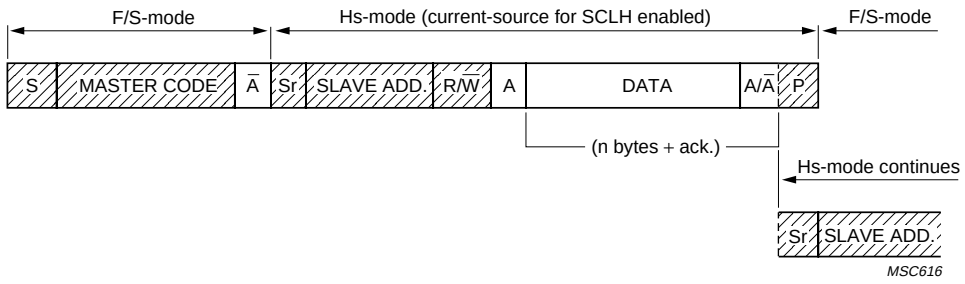


Fig.24 Data transfer format in Hs-mode.

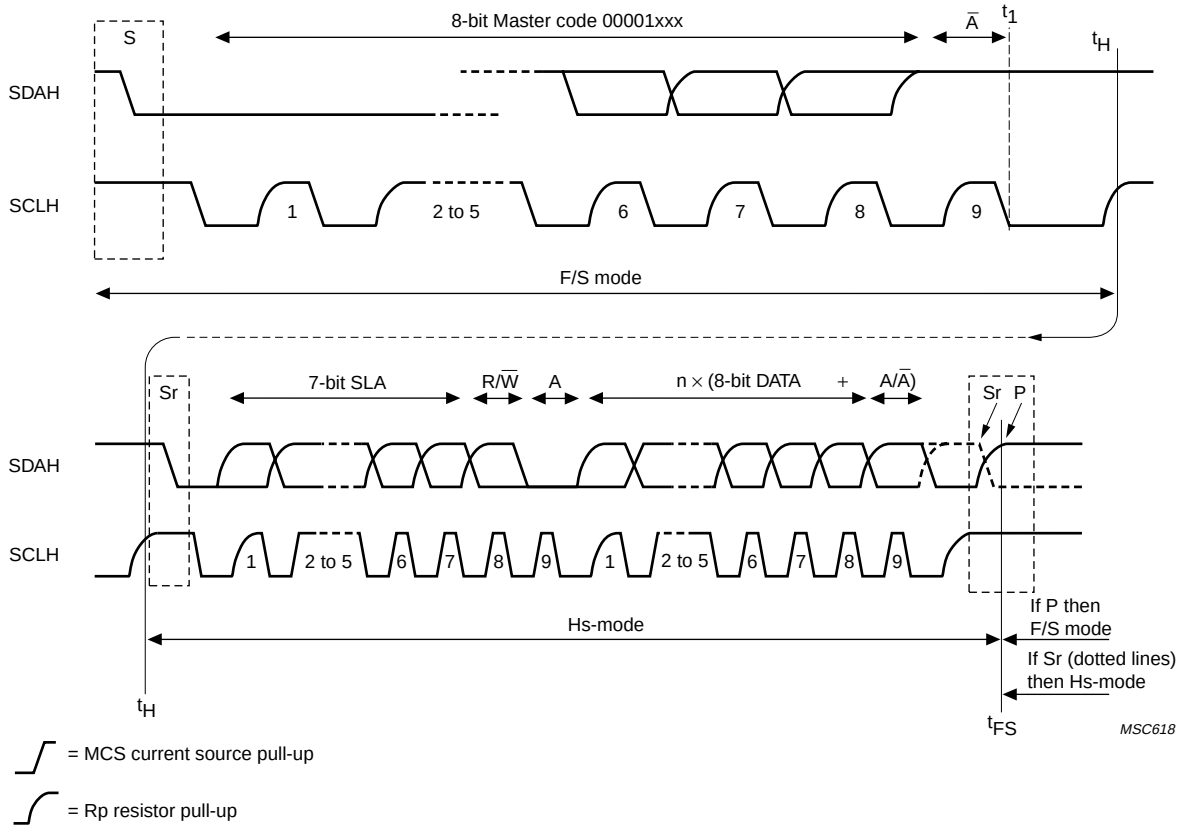


Fig.25 Complete data transfer in Hs-mode.

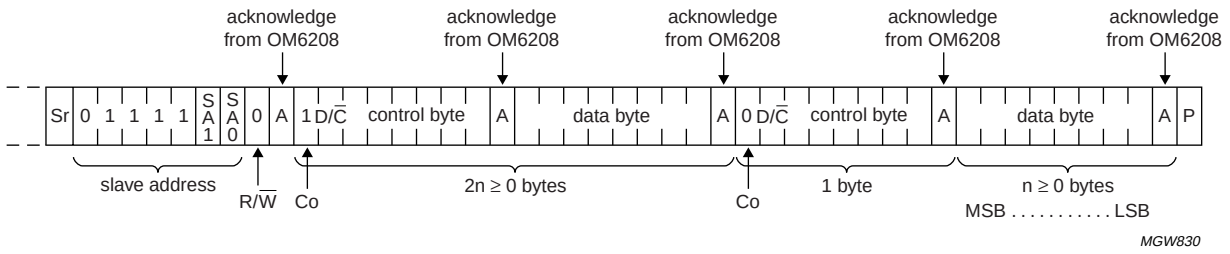
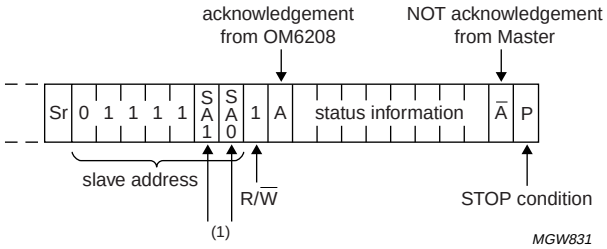


Fig.26 Master transmits in Hs-mode to slave receiver; write mode.



(1) These bits are set by inputs ID3/SA0 and ID4/SA1.

Fig.27 Master receives from slave transmitter (status register is read); read mode.

10.3 Command decoder

The command decoder identifies command words that arrive on the I²C-bus:

- Pairs of bytes
  - first byte determines whether information is display or instruction data
  - 2nd byte contains information.
- Stream of information bytes after Co = 0; display or instruction data depending on last D/$\overline{C}$.

The most-significant bit of a control byte is the continuation bit Co. If this bit is logic 1, it indicates that only one byte, either command or RAM-data, will follow. If this bit is logic 0, it indicates that a series of bytes, either command or RAM-data, may follow. The DB6 bit of a control byte is the RAM-data/command bit D/$\overline{C}$. When this bit is logic 1, it indicates that a RAM-data byte will be transferred next. If the bit is logic 0, it indicates that a command byte will be transferred next.

10.4 Read mode

I²C-bus read mode operates differently from the other interfaces. Two different status bytes can be read back and are selected by first sending a 'read' instruction. A repeated START or STOP and START must then be generated followed by the slave address with the R/W bit set to read in order to read the status register.

Sending the instruction to read ID1, ID2 and VM will select the status byte shown in Table 5.

Sending the instruction to read back the temperature sensor will select the status byte shown in Table 6.

Table 5 Read status byte ID1, ID2 and VM

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
x[1]	x[1]	x[1]	x[1]	x[1]	VM	ID2[2]	ID1[2]

Notes

1. x = undefined.
2. Bits ID3 and ID4 are not available for I²C-bus because they are used to make up the two LSBs of the slave address.

Table 6 Read temperature sensor

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
x[1]	TD[6]	TD[5]	TD[4]	TD[3]	TD[2]	TD[1]	TD[0]

Note

1. x = undefined.

11 INSTRUCTIONS

The OM6208 may be interfaced via 3-line or 4-line Serial Peripheral Interface (SPI), 3-line serial interface or I²C-bus interface. In all cases, processing of instructions is asynchronous and does not require the internal/external oscillator to be running.

Data transmission to OM6208 may be of two types, those that define the operating mode of the device (commands) and those that fill display RAM (data). Table 7 lists all commands that are recognised by OM6208.

The Most Significant Bit (MSB) is sent first. The mode in which the D/$\overline{C}$ bit is defined varies with the type of serial interface that is used.

D/$\overline{C}$ bit definitions:

- With 4-line SPI interface selected, the D/$\overline{C}$ bit is implemented as hard-wired input at pad D/$\overline{C}$
- With 3-line SPI interface selected, the D/$\overline{C}$ bit is not implemented and all transmission are commands by default unless preceded by the Display data length command
- With 3-line serial and I²C-bus interface selected, the D/$\overline{C}$ bit is implemented through the interface protocol.

Commands can consist of one byte (single-byte) and two bytes (double-byte). Unless otherwise specified, commands may be executed in any order.

Table 7 Instruction set

Instructions not expressly defined in this table and reserved instructions must not be used.

COMMAND NAME	D/$\overline{C}$	COMMAND BYTE								FUNCTION DESCRIPTION
		(MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
Write data	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	RAM data
Horizontal addressing	0	0	0	0	0	X_3	X_2	X_1	X_0	set X address; lower 4 bits
Horizontal addressing	0	0	0	0	1	$\delta^{(1)}$	X_6	X_5	X_4	set X address; upper 3 bits
Power control	0	0	0	1	0	1	PC	$\delta^{(1)}$	$\delta^{(1)}$	charge pump on/off
Charge pump control	0	0	0	1	1	1	1	0	1	set multiplication factor
	0	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	S_1	S_0	
Set V_{PR}	0	0	0	1	0	0	V_{pr7}	V_{pr6}	V_{pr5}	write V_{pr} register
Set V_{PR}	0	1	0	0	V_{pr4}	V_{pr3}	V_{pr2}	V_{pr1}	V_{pr0}	write V_{pr} register
Set bias	0	0	0	1	1	0	BS_2	BS_1	BS_0	set bias
Display mode	0	1	0	1	0	0	1	0	DAL	all on/normal display
Display mode	0	1	0	1	0	0	1	1	E	normal/inverse display
Display mode	0	1	0	1	0	1	1	1	DON	display ON/OFF
Data order	0	1	0	1	0	1	0	0	DOR	swap RAM MSB/LSB order
RAM addressing	0	1	0	1	0	1	0	1	V	vertical or horizontal mode
Vertical addressing	0	1	0	1	1	Y_3	Y_2	Y_1	Y_0	set Y address
Vertical addressing	0	0	0	1	1	1	1	1	Y_4	set Y address
Vertical mirroring	0	1	1	0	0	MY	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	mirror Y
ID read	0	1	1	0	1	1	0	1	0	identification: ID1[2][3]
ID read	0	1	1	0	1	1	0	1	1	identification: ID2[2][3]
ID read	0	1	1	0	1	1	1	0	0	identification: ID3[2]
ID read	0	1	1	0	1	1	1	0	1	identification: ID4[2]
Temperature sense	0	1	1	0	1	1	1	1	0	temperature read back
VM read	0	1	1	0	1	1	1	1	1	voltage monitor[3][4]
Row control	0	1	1	1	0	0	0	0	BRS	swap the bottom rows

COMMAND NAME	D/$\overline{C}$	COMMAND BYTE								FUNCTION DESCRIPTION
		(MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
Software reset	0	1	1	1	0	0	0	1	0	internal reset
NOP	0	1	1	1	0	0	0	1	1	no operation
Display data length	0	1	1	1	0	1	0	0	0	display data length for 3-line SPI
	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
Temperature compensation	0	0	0	1	1	1	0	0	0	set TC slopes A and B (SLA and SLB)
	0	$\delta^{(1)}$	SLB_2	SLB_1	SLB_0	$\delta^{(1)}$	SLA_2	SLA_1	SLA_0	
Temperature compensation	0	0	0	1	1	1	0	0	1	set TC slopes C and D (SLC and SLD)
	0	$\delta^{(1)}$	SLD_2	SLD_1	SLD_0	$\delta^{(1)}$	SLC_2	SLC_1	SLC_0	
Frame frequency range, oscillator tune and mode	0	0	0	1	1	1	1	0	0	frame frequency range and oscillator tune and working mode
	0	MOD	T_2	T_1	T_0	$\delta^{(1)}$	FR_2	FR_1	FR_0	
Temperature compensation enable	0	1	1	1	0	1	0	1	TCE	enable/disable temperature compensation
Oscillator selection	0	0	0	1	1	1	0	1	EC	external oscillator
OTP programming	0	1	1	1	1	0	0	OSE	CAL MM	enter calibration mode and control programming
LOAD 0	0	1	1	0	1	1	0	0	0	write 0 to shift register
LOAD 1	0	1	1	0	1	1	0	0	1	write 1 to shift register
Select factory defaults	0	1	1	1	0	1	1	0	SFD	enable/disable defaults
N-line inversion and super-frame inversion	0	1	0	1	0	1	1	0	1	N-line inversion and super-frame Inversion
	0	FI	NL_6	NL_5	NL_4	NL_3	NL_2	NL_1	NL_0	
	0	0	1	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	reserved
	0	1	0	1	0	0	0	$\delta^{(1)}$	$\delta^{(1)}$	reserved
	0	1	0	1	0	1	1	0	0	reserved
	0	1	1	0	1	0	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	reserved
	0	1	1	1	0	1	0	0	1	reserved
	0	1	1	1	0	0	1	$\delta^{(1)}$	$\delta^{(1)}$	reserved
	0	1	1	1	0	1	1	1	$\delta^{(1)}$	reserved
	0	1	1	1	1	0	1	$\delta^{(1)}$	$\delta^{(1)}$	reserved for testing
	0	1	1	1	1	1	$\delta^{(1)}$	$\delta^{(1)}$	$\delta^{(1)}$	reserved for testing

Notes

1. δ = don't care.
2. ID1, ID2, ID3, ID4 and VM are read back via interface as described in Section 9.2.3. Reading back with I^2C-bus interface is possible for temperature, ID1, ID2 and VM, as described in Section 10.4.
3. ID1 will always return to logic 0; ID2 will always return to logic 1. The VM bit is set to logic 1 when the charge pump is running and logic 0 when the charge pump is not running.
4. If the Factory Defaults bit (MMFD) has been programmed to 1, then the SFD instruction is ignored and the device will always use the OTP default data.

11.1 Description of command bits

Table 8 Bit descriptions

BIT	0	1	RESET STATE
DON	display off	display on	0
E	normal display	inverse video mode	0
DAL	normal display	all pixel on	1
MY	no Y mirroring	Y mirroring	0
PC	charge pump off	charge pump on	0
DOR	normal data order	MSB/LSB transposed for RAM data	0
V	horizontal addressing	vertical addressing	0
BRS	bottom rows are not mirrored	bottom rows are mirrored	0
EC	internal oscillator is selected	external clock to be used	0
CALMM	exit OTP calibration mode	enter OTP calibration mode(1)	0
TCE	disable temperature compensation	enable temperature compensation	1
OSE	disable OTP programmed voltage	enable OTP programmed voltage(1)	0
SFD	use interface programmed data	use OTP programmed data(2)	0
MOD	grey-scale mode is selected	black-and-white mode is selected	0
SLA[2:0]	select slope for segment A		000(2)
SLB[2:0]	select slope for segment B		000(2)
SLC[2:0]	select slope for segment C		000(2)
SLD[2:0]	select slope for segment D		000(2)
X[6:0]	sets X address (column) for writing in the RAM		0000000
Y[4:0]	sets Y address (bank) for writing in the RAM		00000
S[1:0]	charge pump multiplication factor (see Table 10)		0000(2)
NL[6:0]	sets N-line inversion (see Table 18)		0001101(2)
FR[2:0]	sets frame frequency range (see Table 11)		001(2)(3)
T[2:0]	oscillator tune; sets frame frequency within a range (see Table 11)		110(2)(3)
D[7:0]	display data length for 3-line SPI interface		00000000
VPR[7:0]	V_{PR} register		00000000(2)
BS[2:0]	bias setting level (see Table 13)		000(2)
FI	super-frame inversion		0(2)

Notes

1. Calibration mode may not be entered if the SEAL bit has been set. Programming is only possible when in calibration mode.
2. These values can be set by the module maker. If the factory defaults OTP bit (MMFD) has been set then these values cannot be changed via the interface. Otherwise, the OTP data will only be used if bit SFD is set to 1.
3. FR[2:0] = 001 and T[2:0] = 110 gives 150 Hz as default frame frequency.

Table 9 Display and power mode bits DON, DAL and E

DON	DAL[1]	E[2]	DESCRIPTION
0	0	X[3]	display off; all row and column outputs at V_{SS}; oscillator on; HV generator enabled
0	1	X[3]	Power-down mode; display off; all row and column outputs at V_{SS}; oscillator off; HV generator disabled
1	0	0	normal display mode
1	0	1	inverse display mode
1	1	X[3]	all pixels on

Notes

1. The DAL bit has priority over the $\overline{E}$ bit.
2. Refer also to Table 17.
3. X = don't care.

Table 10 Multiplication settings for charge pump

S1	S0	VOLTAGE MULTIPLIER
0	0	4 ×
0	1	5 ×
1	0	6 ×
1	1	7 ×

11.2 Frame frequency setting and oscillator tuning

Grey-scale mode and black-and-white mode require different frame frequencies. The appropriate frame frequency (f_{frame}) is derived from the oscillator frequency (f_{osc}) using a presettable divider as shown in the equation

$$f_{frame} = \frac{f_{OSC}}{\text{division ratio}}$$

There are eight possible divider settings and these are selected by the parameter FR[2:0], see Table 11.

Table 11 Frame frequencies for f_{osc} = 400 kHz

FR2	FR1	FR0	DIVISION RATIO	f_{frame} (Hz)
0	0	0	2448	163.4
0	0	1	3265	122.5
0	1	0	4082	98.0
0	1	1	4896	81.7
1	0	0	5714	70.0
1	0	1	7340	54.5
1	1	0	8968	44.6
1	1	1	11428	35.0

Oscillator tuning is controlled by the parameter T[2:0]. As a result of oscillator tuning, f_{OSC} is increased by approximately 4% per step according to the equation

$$f_{OSC} = 400\ \text{kHz} \times (1 + 0.04 \times T) \quad (1)$$

where T is the decimal value of T[2:0].

Example. For the default values given in Table 8 (i.e. FR[2:0] = 001 and T[2:0] = 110) the selected frame frequency is 122.5 Hz × (1 + 6 × 0.04) = 151.9 Hz.

Equation (1) shows the typical value of the oscillator frequency. The accuracy of this parameter is defined in Chapter 15. The frame frequency accuracy results directly from the oscillator accuracy.

11.3 Initialization

Immediately following power-on, all internal registers and the RAM content are undefined. A reset pulse must be applied to the $\overline{RES}$ pad.

Reset is accomplished by applying an external reset pulse (active LOW) to the $\overline{RES}$ input. When reset occurs within the specified time, all internal registers are reset, however the RAM remains undefined. The state after reset is described in Section 11.4.

At power-on, the $\overline{RES}$ input must be $\leq 0.3V_{DD1}$ when V_{DD1} reaches $V_{DD(min)}$ (or higher) within the maximum time t_{VHRL} after V_{DD1} going HIGH (see Fig.37). Alternatively a reset pulse can be applied when V_{DD1} is stable.

A reset can also be made by sending a reset command. This command can be used during normal operation but not to initialize the chip after power-on.

After power-off, the $\overline{RES}$ input must not be HIGH when V_{DD1} is not HIGH.

11.4 Reset function

After reset, the LCD driver is in Power-down mode, the RAM is undefined and the internal registers have the status shown in Table 8.

11.5 Power-down mode

In the Power-down mode:

- All LCD outputs (row and column outputs) are at V_{SS} (display off)
- Bias generator and V_{LCD} generator are switched off; external V_{LCD} supply can be applied or disconnected
- Oscillator is off (an external clock is possible)
- RAM contents are unchanged; RAM data can be written
- V_{LCD} is discharged to V_{SS}.

Power-down mode is active when the display is off (DON = 0) and all the pixels are on (DAL = 1).

11.6 Display Control

The bits DON, E and DAL select the display mode (see Table 9).

11.6.1 Horizontal mirroring

When the MX input is at logic 0, the display RAM is written from left to right (X = 0 is on the left side).

When the MX input is set to 1, the display RAM is written from right to left (X = 0 is on the right side).

The MX input value has an impact on the way the RAM is written: if a horizontal mirroring of the display is desired, the RAM must be rewritten after changing the MX pad value.

11.6.2 Vertical mirroring

When the MY bit is set to logic 1, the display is mirrored vertically.

A change of this bit has an immediate effect on the display, it is not necessary to rewrite RAM for the effect to take place.

11.7 Set Y address of RAM

Y[4:0] defines the Y address of the display RAM.

Table 12 Y address range

Y4	Y3	Y2	Y1	Y0	DISPLAY RAM
0	0	0	0	0	bank 0
0	0	0	0	1	bank 1
0	0	0	1	0	bank 2
0	0	0	1	1	bank 3
0	0	1	0	0	bank 4
0	0	1	0	1	bank 5
0	0	1	1	0	bank 6
0	0	1	1	1	bank 7
0	1	0	0	0	bank 8
0	1	0	0	1	bank 9
0	1	0	1	0	bank 10
0	1	0	1	1	bank 11
0	1	1	0	0	bank 12
0	1	1	0	1	bank 13
0	1	1	1	0	bank 14
0	1	1	1	1	bank 15
1	0	0	0	1	bank 16

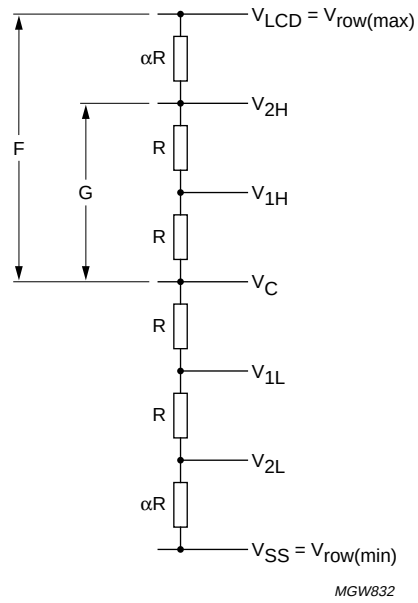
11.8 Set X address of RAM

The X address points to the columns. The range of X is 0 to 95.

11.9 Bias levels

The OM6208 is a grey-scale driver able to provide different bias voltage levels for rows and columns. The row voltage values are V_{LCD}, V_{SS} and V_C, generated using the resistor chain shown in Fig.28.

The five levels used to drive the columns are shown in Fig.28. These are V_{2L}, V_{1L}, V_C, V_{1H} and V_{2H}, all of which depend on the value of alpha. Table 13 shows all possible combinations of alpha settable by programming the BS[2:0] bits.



α is in the range 0.0 to 1.05.

Fig.28 Bias system.

Table 13 Bias setting levels for p = 4

BS2	BS1	BS0	F/G	α	a
0	0	0	1.000	0.00	4.00
0	0	1	1.075	0.15	4.30
0	1	0	1.150	0.30	4.60
0	1	1	1.225	0.45	4.90
1	0	0	1.300	0.60	5.20
1	0	1	1.375	0.75	5.50
1	1	0	1.450	0.90	5.80
1	1	1	1.525	1.05	6.10

Each of the eight possible values of alpha results in a different set of five values for the column voltages.

Bias level F (see Fig.28) is half of the maximum row voltage level as shown by the equation

$$F = \frac{V_{LCD}}{2}$$

Figure 28 also shows that G is used to define the maximum column voltage level related to the V_C level.

Because the voltage level of the row depends on the programmed bias level, it can be seen that $F \geq G$

The situation where F = G occurs only when BS[2:0] is zero and alpha is zero. In this case αR = 0 and G = F; therefore $V_{2H} = V_{LCD}$ and $V_{2L} = V_{SS}$, also two of the internal buffers are no longer needed and therefore are switched off to reduce power consumption.

The relationship between F and G is defined by the parameter a (indicated in Table 13) and p as follows

$$\frac{F}{G} = \frac{a}{p}$$

It can be seen from Fig.28 that

$$\frac{F}{G} = \frac{a}{p} = \frac{(\alpha + 2)}{2} = 1 + \frac{\alpha}{2}$$

or

$$a = \left(\frac{\alpha}{2} + 1\right) \cdot p \qquad \alpha = \left(\frac{a}{p} - 1\right) \cdot 2$$

The BS[2:0] bias bits can be selected by a command and also can be programmed by OTP.

The relationship between the parameters F, p, a and N (number of rows of the display) and the $V_{on(rms)}$ and $V_{off(rms)}$ voltage values according to the typical LCD properties of the pixel are shown in equations (2) and (3).

$$V_{on(rms)} = \frac{F}{a} \cdot \sqrt{\frac{p \cdot (a^2 + N + 2a)}{N}} \quad (2)$$

$$V_{off(rms)} = \frac{F}{a} \cdot \sqrt{\frac{p \cdot (a^2 + N - 2a)}{N}} \quad (3)$$

11.10 LCD drive voltage

11.10.1 LCD DRIVE VOLTAGE GENERATION

V_{LCD} may be supplied externally or generated internally by the on-chip capacitive charge pump. OM6208 features on-chip capacitors resulting in a minimum of external components required for operation (see Chapter 16).

The 'power control' instruction may be used to switch V_{LCD} generation on or off. The charge pump control instruction may be used to select the required voltage multiplication factor. The 'set V_{PR}' instruction is used for programming the LCD drive voltage V_{LCD}.

The generation of V_{LCD} in OM6208 is illustrated in Fig.29. This shows all factors that effect V_{LCD} generation, including the 6 bits of MMVOPCAL (from OTP) and the 7 bits resulting from the temperature compensation mechanism. Equations summarizing all factors are

$$V_{OP} = V_{PR} + MMVOPCAL + V_T \quad (4)$$

and

$$V_{LCD} = V_{OP} \cdot b + a \quad (5)$$

Where:

V_{PR}[7:0] is set in the instruction decoder and is the programmed V_{PR} register value as an unsigned number

MMVOPCAL[5:0] is the value of the offset stored in the OTP cells in twos complement format

V_T[7:0] in twos complement format comes from the temperature compensation block (see Table 16)

a and b are fixed constant values (see Table 14).

Table 14 Parameters of V_{LCD}

SYMBOL	VALUE	UNIT
b	0.03	V
a	3	V

CAUTION
As the programming range for the internally generated V_{LCD} allows values above the maximum allowed V_{LCD} (9 V), the user has to ensure, while setting the V_{PR} register and selecting the temperature compensation, that under all conditions and including all tolerances V_{LCD} remains below 9.0 V. Also, because the programming range for the internally generated V_{LCD} allows values below the minimum allowed V_{LCD} (5 V), the user has to ensure, while setting the V_{PR} register and selecting the temperature compensation, that under all conditions and including all tolerances V_{LCD} remains above 5.0 V.

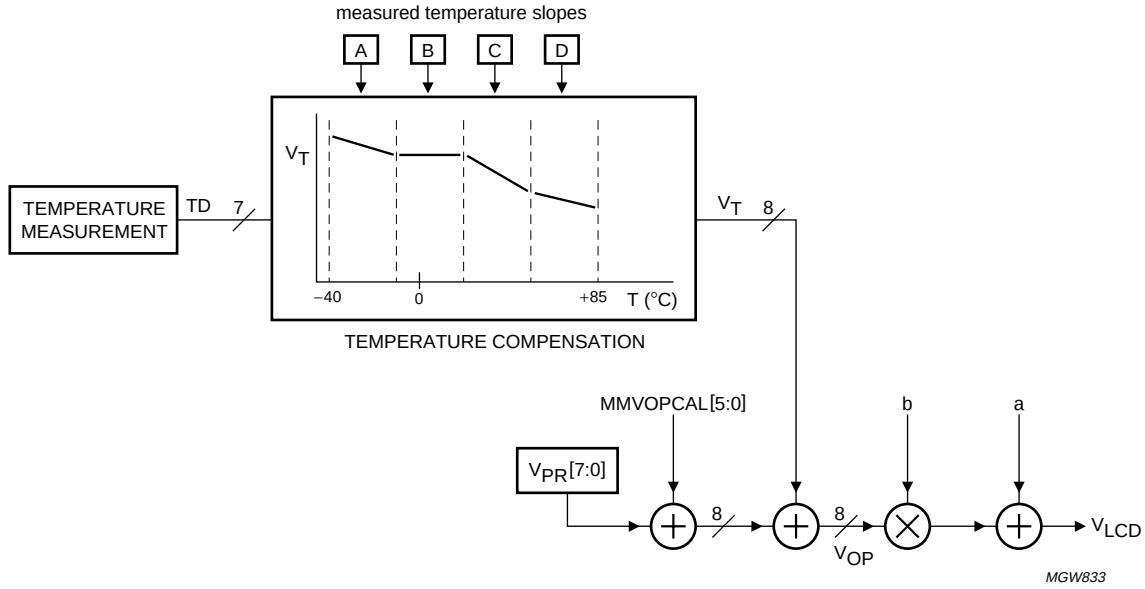
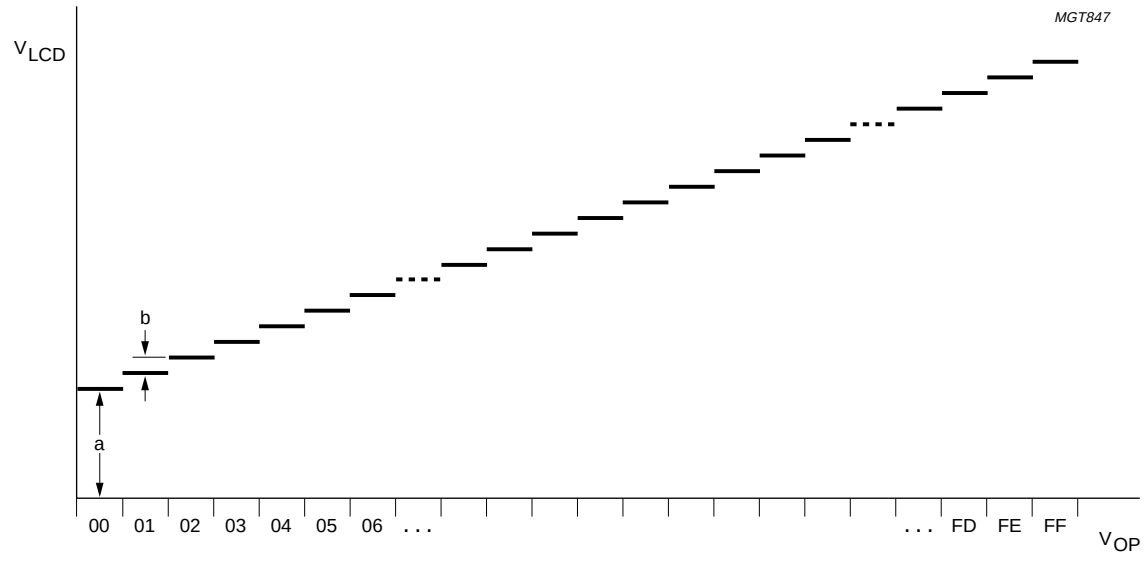


Fig.29 V_{LCD} generation including the temperature compensation and OTP calibration.



V_{PR}[7:0] programming: 00 to FF (HEX).
Assuming MMVOPCAL = 0 and V_T = 0 V.

Fig.30 V_{LCD} programming of OM6208 shown as plots of equations (4) and (5).

11.10.2 Temperature measurement

The temperature measurement is repeated every 10 seconds. The measured value is provided as a 7-bit digital value TD[6:0] which can be read back via the interface. The temperature can be determined from TD[6:0] using the equation

$$T = (1.875 \times TD - 40)°C \quad (6)$$

11.10.3 Temperature compensation

Due to the temperature dependency of the liquid crystal's viscosity, the LCD controlling voltage V_{LCD} may have to be adjusted at different temperatures to maintain optimal contrast.

Internal temperature compensation may be enabled via the 'temperature compensation enable' instruction. When the internal temperature compensation is applied (TCE bit is set to 1) then according to Equation (4) the V_{LCD} depends also on V_T (the temperature compensation component defined in Table 16), otherwise V_T is considered to be 0 V.

After the reset, the V_{LCD} is fixed because the V_{PR} is a register that is reset to zero. The MMVOPCAL is also set to zero because this comes from the registers of OTP that are not refreshed yet, also V_T is evaluated after the reset because the temperature measurement block supplies a TD value that is the default value stored in the register after the reset.

The four temperature coefficients MA, MB, MC and MD correspond to four equally spaced temperature regions. Each coefficient can be selected from a choice of eight different slopes, or multiplication factors. Each one of these coefficients may be independently selected by the user via the 'temperature compensation enable' instruction. The default for each slope register can be stored in OTP.

Table 15 Temperature coefficients

Slopes of V_{LCD} are calculated from equations (4), (5), (6) and Table 16.

SLA, SLB, SLC and SLD	MA, MB, MC and MD	SLOPE (mV/K)
111	3.00	–48
110	2.00	–32
101	1.25	–20
100	1.00	–16
011	0.75	–12
010	0.50	–8
001	0.25	–4
000	0.00	0

Temperature compensation is implemented by adding an offset V_T to the V_{PR} value (additionally to the OTP calibration offset MMVOPCAL).

The final result for V_{LCD} calculation is an 8-bit positive number as shown in equations (4) and (5). Care must be taken by the user to ensure that the ranges of V_{PR}, MMVOPCAL and V_T do not cause clipping and hence undesired results. The adder stages will not permit overflow or underflow and will clamp results to either end of the range.

The temperature read-out generates a 7-bit result, TD[6:0]. For temperatures below –40 °C, the value of TD is zero. For temperatures above 79 °C, the value of TD is higher than 63, but for V_T calibration the value TD = 63 is used.

The offset value V_T may be calculated from Table 16. The effect on V_{LCD} can be calculated by multiplying the offset value with the value of b (from Table 14).

For example, if T = –10 °C, TD = 16 and MB = 1.25 then $V_{LCDoffset}$ = 30 mV × (32 – 16) × 1.25 = 600 mV.

Table 16 Temperature compensation equations

TEMPERATURE RANGE (°C)	TD RANGE	EQUATION
–40 to –11	0 to 15	$V_T = (16 \times MB) + MA \times (16 - TD)$
–10 to +19	16 to 31	$V_T = (32 - TD) \times MB$
+20 to +49	32 to 47	$V_T = -(TD - 32) \times MC$
+50 to +79	48 to 63	$V_T = -(16 \times MC) + MD \times (TD - 48)$

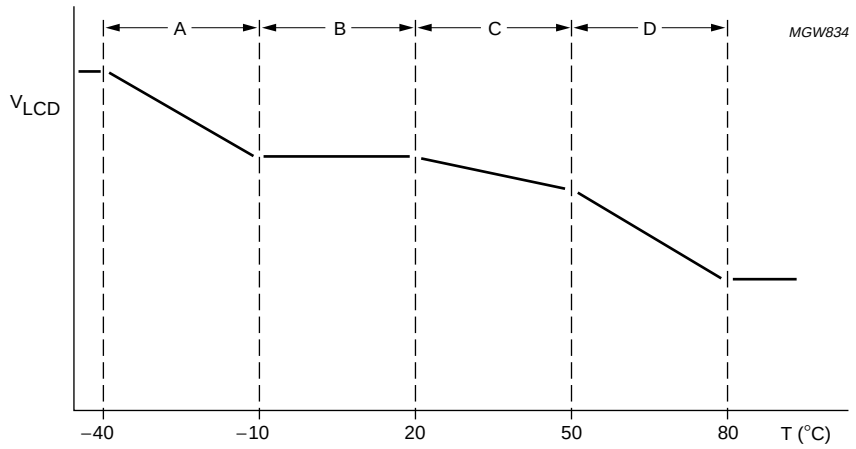


Fig.31 Example of segmented temperature coefficients.

11.11 Grey-scale mode and black-and-white mode

It is possible to set via command the working mode of the OM6208. This is by setting the MOD bit of the 'frame frequency' instruction, oscillator tune and mode.
By default, the MOD bit is set to logic 0 and grey-scale mode is selected. In that mode, grey-scales are generated using Frame Rate Control (FRC). Three frames together form a super-frame. The frame frequency is adjustable but all three frames have the same duration. A grey-scale is generated by selecting either 0, 1, 2 or all 3 frames (see Table 17).

If the MOD bit is set to logic 1 black-and-white mode is selected, meaning that only black-and-white levels are generated and only one frame type is sent to the display. Thus only the MSBs stored in the RAM are used for all three frames. The LSBs are ignored. Thus the way the data is stored in the RAM is the same as for grey-scale. As all frames are identical the frame frequency may be reduced (see Table 11).

Table 17 Grey-scale levels with FRC

GS[1:0]		SUPER-FRAME(1)	GREY-SCALE LEVELS
Normal mode (E = 0)			
0	0	000	white
0	1	001	light grey
1	0	110	dark grey
1	1	111	black
Inverse mode (E = 1)			
0	0	111	black
0	1	110	dark grey
1	0	001	light grey
1	1	000	white

Note

1. The first and second frames in each super-frame are related to the MSB of GS[1:0] (GS = 11); the third frame is related to the LSB (GS = 00).

11.12 N-line inversion and frame inversion

N-line inversion can be set from 0 to 127 as shown in Table 18.

Table 18 N-line inversion

INVERSION AFTER	NL_6	NL_5	NL_4	NL_3	NL_2	NL_1	NL_0	FI
0-line inversion	0	0	0	0	0	0	0	0
1-line inversion	0	0	0	0	0	0	1	0
2-line inversion	0	0	0	0	0	1	0	0
3-line inversion	0	0	0	0	0	1	1	0
4-line inversion	0	0	0	0	1	0	0	0
5-line inversion	0	0	0	0	1	0	1	0
6-line inversion	0	0	0	0	1	1	0	0
7-line inversion	0	0	0	0	1	1	1	0
8-line inversion	0	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
66-line inversion	1	0	0	0	0	1	0	0
67-line inversion	1	0	0	0	0	1	1	0
68-line inversion	1	0	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:
127-line inversion	0	1	0	0	0	0	0	0
0 only super-frame inversion	0	0	0	0	0	0	0	1
1-line inversion and super-frame inversion	0	0	0	0	0	0	1	1
2-line inversion and super-frame inversion	0	0	0	0	0	1	0	1
3-line inversion and super-frame inversion	0	0	0	0	0	1	1	1
4-line inversion and super-frame inversion	0	0	0	0	1	0	0	1
5-line inversion and super-frame inversion	0	0	0	0	1	0	1	1
6-line inversion and super-frame inversion	0	0	0	0	1	1	0	1
7-line inversion and super-frame inversion	0	0	0	0	1	1	1	1
8-line inversion and super-frame inversion	0	0	0	1	0	0	0	1
:	:	:	:	:	:	:	:	:
66-line inversion and super-frame inversion	1	0	0	0	0	1	0	1
67-line inversion and super-frame inversion	1	0	0	0	0	1	1	1
68-line inversion and super-frame inversion	1	0	0	0	1	0	0	1
:	:	:	:	:	:	:	:	:
127-line inversion and super-frame inversion	1	1	1	1	1	1	1	1

Notes

1. In grey-scale mode the super-frame inversion is performed if bit FI in the ‘N-line inversion and super-frame inversion’ instruction is set to logic 1. In black-and-white mode, the super-frame inversion continues in groups of three frames.
2. NL[6:0] may be set in the range 0 to 127. If NL = 0, then no line inversion is performed; if NL = MUX rate = 68 then N-line inversion is equal to frame inversion.
3. With N-line inversion the output signal polarity changes every N row pulse periods (with p = 4 this means inversion occurs after every $4 \times$ NL rows of the display).
4. If after a super-frame FI = 1 and there is an inversion due to an N-line inversion, this inversion occurs only once.

The example in Table 19 shows the first super-frame with the settings NL = 3, MUX = 20 and p = 4 applied; the super-frame contains three frames. The next super-frame will be a repeat of the first super-frame if bit FI is set to logic 0 (no super-frame inversion), or will start with the first frame having the opposite sign if bit FI is at logic 1 (super-frame inversion) and the N-line inversion counter will also restart.

Super-frame inversion requires that the state of the previous super-frame is remembered, i.e., if the previous super-frame started ‘+’, then the next super-frame must start ‘–’. This has priority over inversions triggered by the counter, so that if the counter triggers an inversion at a super-frame boundary and super-frame inversion is active, then the two do not cancel each other out but the super-frame inversion has priority.

Table 19 Example showing line inversions in one super-frame: NL = 3, MUX = 20 and p = 4

SUPER-FRAME 1																																																											
FRAME 1																				FRAME 2																				FRAME 3																			
SUB FRAME 0					SUB FRAME 1					SUB FRAME 2					SUB FRAME 3					SUB FRAME 0					SUB FRAME 1					SUB FRAME 2					SUB FRAME 3					SUB FRAME 0					SUB FRAME 1					SUB FRAME 2					SUB FRAME 3				
+					–					–					–					+					+					+					–					–					–					+					+				
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12 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); notes 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD1}	supply voltage (logic circuits)	–0.5	+6.5	V
V_{DD2}, V_{DD3}	supply voltage (analog circuits)	–0.5	+5.0	V
V_{LCD}	LCD supply voltage	–0.5	+10.0	V
V_I	input voltage (any pad)	–0.5	V_{DD1} + 0.5	V
I_{SS}	ground supply current	–50	+50	mA
I_I, I_O	DC input or output current	–10	+10	mA
P_{tot}	total power dissipation	–	300	mW
P/out	power dissipation per output	–	30	mW
T_{stg}	storage temperature	–65	+150	°C

Notes

1. Stresses above those listed under limiting values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

13 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

14 DC CHARACTERISTICS

V_{DD1} = 1.7 to 3.3 V; V_{SS} = 0 V; V_{LCD} = 5 to 9.0 V; T_{amb} = –40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD1}	supply voltage (logic circuits)		1.7	–	3.3	V
V_{DD2}, V_{DD3}	supply voltage (analog circuits)		2.4	–	4.5	V
V_{LCDIN}	LCD supply voltage input	LCD voltage supplied externally; high voltage generator disabled	–	–	9.0	V
V_{LCDOUT}	LCD supply voltage output	LCD voltage generated internally; high voltage generator enabled; note 1	–	–	9.0	V
$V_{LCD(tol)}$	tolerance of generated V_{LCD}	with calibration; note 2	–70	–	+70	mV
I_{DD}	supply current; pins V_{DD1}, V_{DD2} and V_{DD3}	Power-down mode (all static currents switched off); note 3	–	3	–	µA
I_{DD1}	supply current; pin V_{DD1}	notes 3 and 4	–	20	40	µA
I_{DD2}, I_{DD3}	supply current; pins V_{DD2} and V_{DD3}	notes 3 and 4				
		DC load on V_{LCD} = 300 µA	–	2400	–	µA
		DC load on V_{LCD} = 170 µA	–	1200	2000	µA
I_{DD2}	supply current; pin V_{DD2}	notes 4 and 5				
		DC load on V_{LCD} = 32 µA	–	360	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Logic circuits						
V_{OL}	LOW-level output voltage	I_{OL} = 0.5 mA	V_{SS}	–	$0.2V_{DD1}$	V
V_{OH}	HIGH-level output voltage	I_{OH} = –0.5 mA	$0.8V_{DD1}$	–	V_{DD1}	V
V_{IL}	LOW-level input voltage		V_{SS}	–	$0.3V_{DD1}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD1}$	–	V_{DD1}	V
I_L	leakage current	$V_I = V_{DD1}$ or V_{SS}	–1	–	+1	μA
Column and row outputs						
R_{col}	column output resistance C0 to C95	V_{LCD} = 7 V	–	3	7	kΩ
R_{row}	row output resistance R0 to R64	V_{LCD} = 7 V; load 10 μA; outputs tested one at a time	–	2	5	kΩ
V_{col}	bias tolerance C0 to C95		–70	0	+70	mV
V_{row}	bias tolerance R0 to R64		–70	0	+70	mV
Temperature read-back						
ΔT_{RB}	temperature read-back tolerance		–8	–	+8	°C

Notes

1. The maximum possible V_{LCD} voltage that may be generated is dependent on voltage, temperature and (display) load.
2. Valid for the values of temperature, V_{PR} and temperature compensation used at calibration.
3. V_{DD1} = 1.8 V; V_{DD2} = 2.7 V; inputs at V_{DD1} or V_{SS}; interface inactive; internal V_{LCD} generation.
4. Grey-scale or black-and-white mode; display mode ON; all outputs open-circuit; BS[2:0] = 000.
5. V_{LCD} = 6.84 V; default frequency; data pattern in RAM is with all bytes = AA(HEX); multiplication factor = 5.

15 AC CHARACTERISTICS

V_{DD1} = 1.7 to 3.3 V; V_{SS} = 0 V; V_{LCD} = max. 9.0 V; T_{amb} = –40 to +85 °C; all timings are between 20% and 80% of V_{DD1}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{OSC}	oscillator frequency selection	see Section 11.2, equation (1)	400(1)	496(2)	512(3)	kHz
f_{EXT}	external clock frequency		400	496	512	kHz
f_{frame}	frame frequency selection	default frequency: FR[2:0] = 001; T[2:0] = 110	35	151.9	210	Hz
Δf_{OSC}, Δf_{frame}	accuracy of oscillator frequency and frame frequency	V_{DD1} = 2.8 V; T_{amb} = –20 to +70 °C	–15	–	+15	%
Serial timing characteristics: 3-line and 4-line SPI and serial interface; V_{DD1} = 1.8 to 3.3 V; see Figs 32 to 35						
f_{SCLK}	clock frequency		–	–	6.5	MHz
T_{CYC}	SCLK clock cycle time		153	–	–	ns
t_{PWH1}	SCLK pulse width high		70	–	–	ns
t_{PWL1}	SCLK pulse width low		60	–	–	ns
t_{S2}	$\overline{SCE}$ set-up time		60	–	–	ns
t_{H2}	$\overline{SCE}$ hold time		60	–	–	ns
t_{PWH2}	$\overline{SCE}$ minimum HIGH time		50	–	–	ns
t_{S4}	SDATA set-up time		60	–	–	ns
t_{H4}	SDATA hold time		60	–	–	ns
t_{S3}	data/$\overline{command}$ set-up time		60	–	–	ns
t_{H3}	data/$\overline{command}$ hold time		60	–	–	ns
t_{S1}	SDATA set-up time		50	–	–	ns
t_{H1}	SDATA hold time		70	–	–	ns
t_1	SDO access time		–	–	50	ns
t_2	SDO disable time	3-line SPI or 4-line SPI interface	–	–	50	ns
t_3	SCE hold time		50	–	–	ns
t_4	SDO disable time	3-line serial interface	25	–	110	ns
C_b	capacitive load for SDO	note 4	–	–	50	pF
R_b	series resistance for SDO	note 4	–	–	500	Ω
I²C-bus interface timing characteristics; V_{DD1} = 1.8 to 3.3 V; see Fig.36						
f_{SCLH}	SCLH clock frequency		0	–	3.4	MHz
$t_{SU;STA}$	set-up time (repeated) START condition		160	–	–	ns
$t_{HD;STA}$	hold time (repeated) START condition		160	–	–	ns
t_{LOW}	LOW period of the SCLH clock		160	–	–	ns
t_{HIGH}	HIGH period of the SCLH clock		60	–	–	ns
$t_{SU;DAT}$	data set-up time		10	–	–	ns
$t_{HD;DAT}$	data hold time		15	–	70	ns
t_{rDA}	rise time of SDAH signal		20	–	80	ns
t_{fDA}	fall time of SDAH signal		20	–	80	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{SU;STO}$	set-up time for STOP condition		160	–	–	ns
C_b	capacitive load for SDAH and SCLH lines	note 5	–	–	100	pF
	capacitive load for SDAH + SDA line and SCLH + SCL line		–	–	400	pF
t_{SW}	tolerable spike width on bus		–	–	5	ns
V_{nL}	noise margin at the LOW level for each connected device (including hysteresis)		$0.1V_{DD}$	–	–	V
V_{nH}	noise margin at the HIGH level for each connected device (including hysteresis)		$0.2V_{DD}$	–	–	V
RESET timing characteristics; see Fig.37						
t_{VHRL}	V_{DD} to $\overline{RES}$ LOW		0[6]	–	1	µs
t_{RW}	reset low pulse width		1000	–	–	ns
t_{RWS}	reset pulse width spike suppression		–	–	100	ns

Notes

1. f_{OSC} defined for T[2:0] = 000.
2. f_{OSC} defined for T[2:0] = 110 (default value).
3. f_{OSC} defined for T[2:0] = 111.
4. Maximum value is for f_{SCLK} = 6.5 MHz; series resistance includes ITO track + connector resistance + PCB.
5. C_b = 100 pF total capacitance of one bus line.
6. $\overline{RES}$ may be LOW before V_{DD1} goes HIGH.

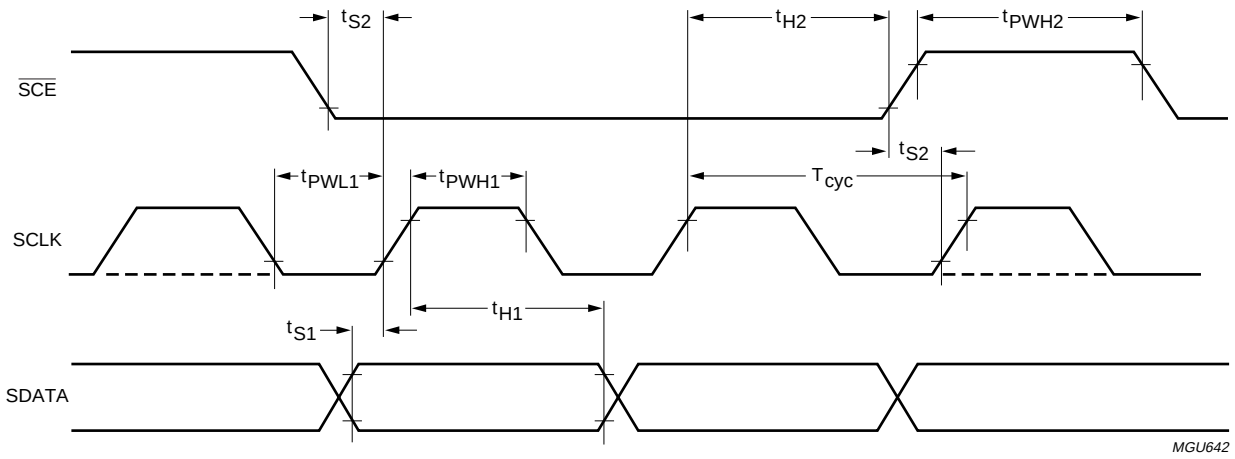


Fig.32 3-line serial interface timing.

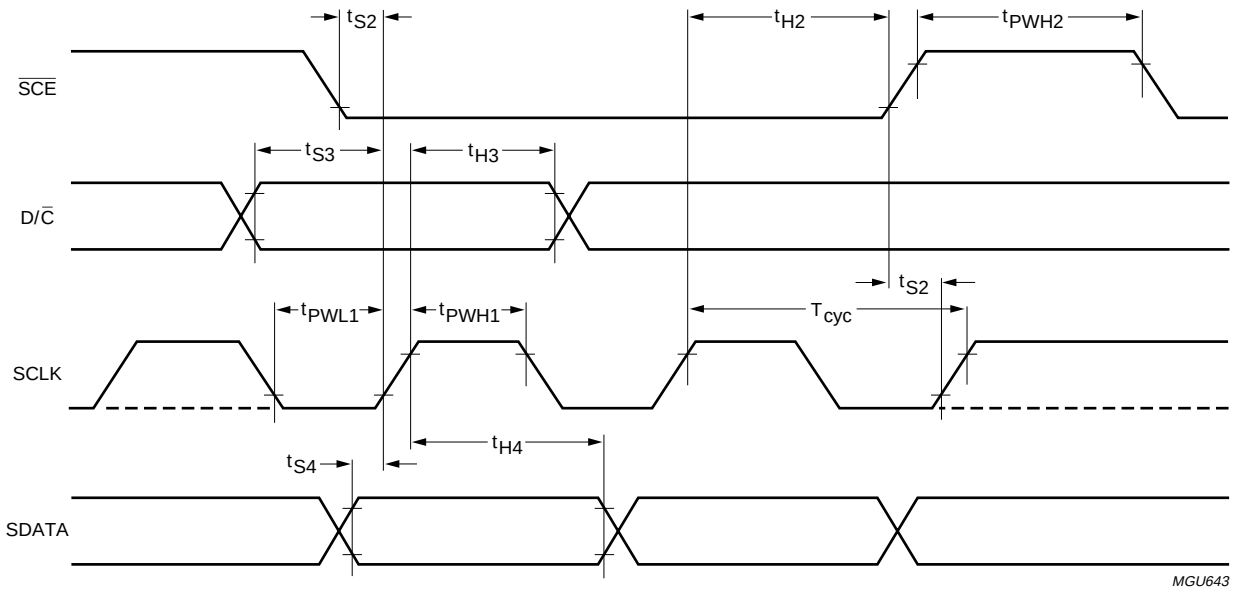


Fig.33 4-line SPI interface timing.

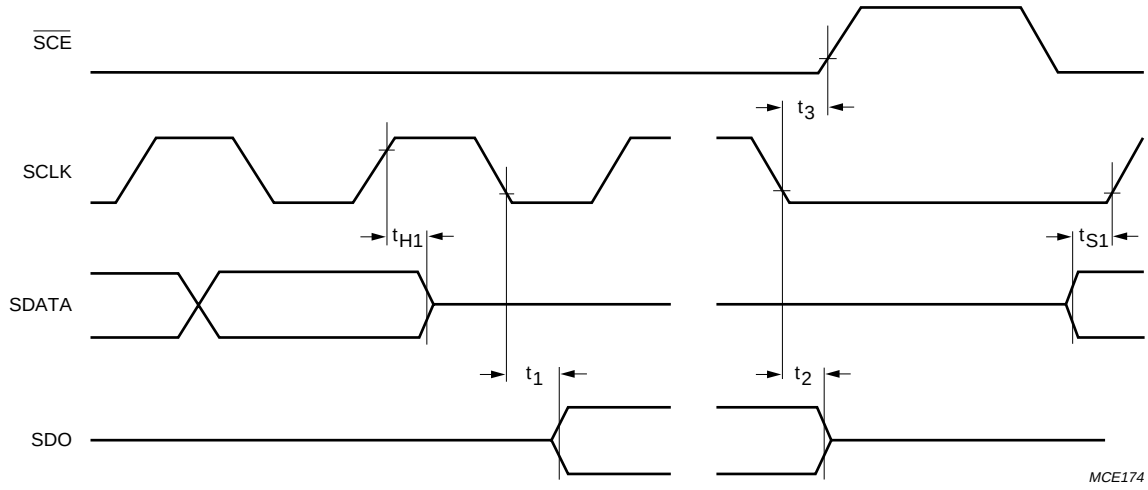


Fig.34 3-line and 4-line SPI timing (read mode).

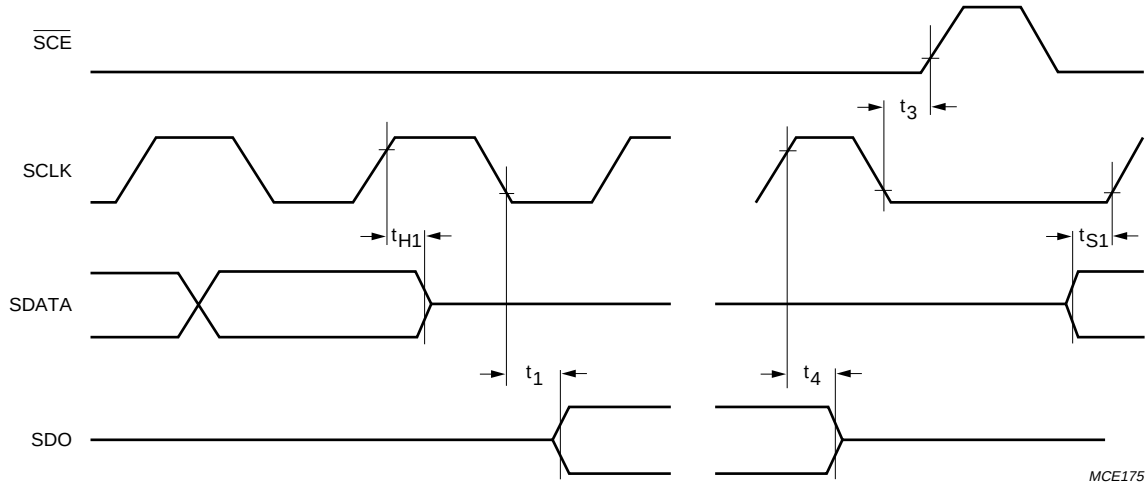


Fig.35 3-line serial interface timing (read mode).

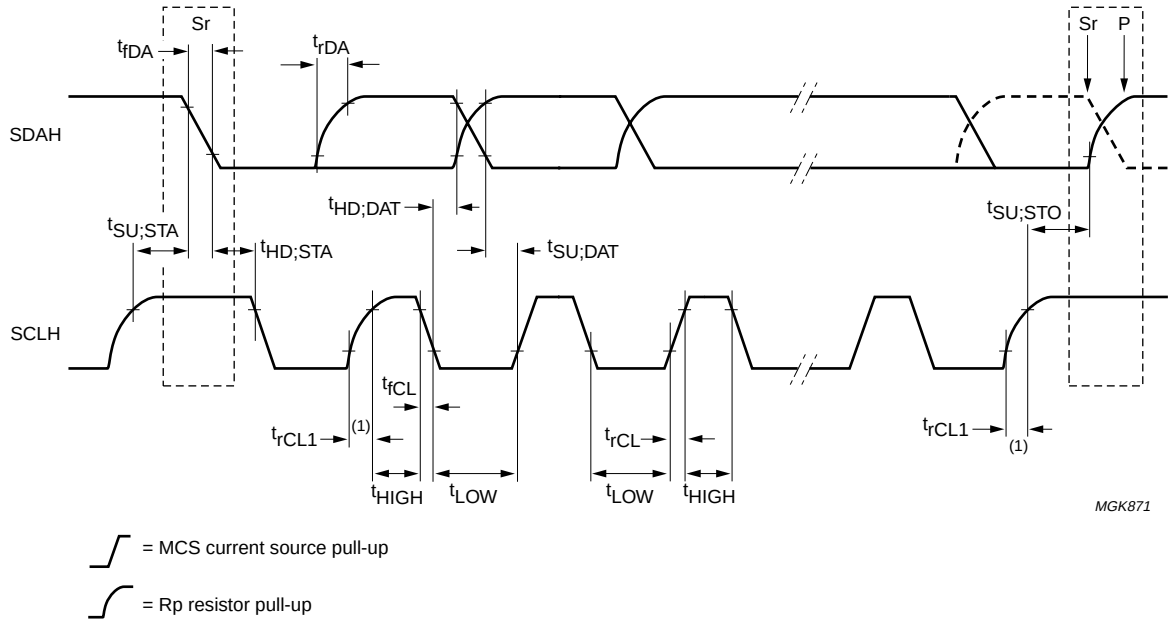


Fig.36 I²C-bus timing diagram (Hs-mode).

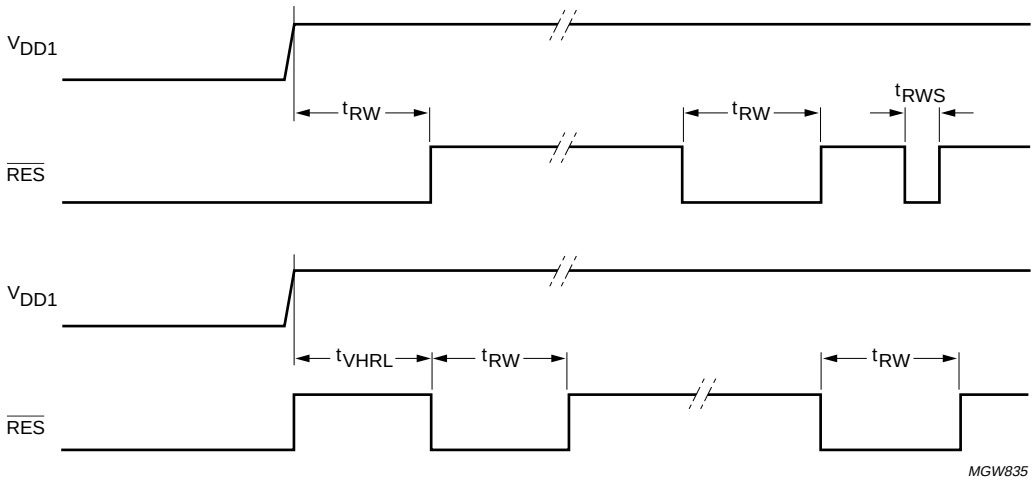


Fig.37 Reset timing.

16 APPLICATION INFORMATION

16.1 Protection from light

Semiconductors are light sensitive. Exposure to light sources can cause malfunction of the IC. In the application it is therefore required to protect the IC from light. The protection has to be done on all sides of the IC, i.e. front, rear and all edges.

16.2 Chip-on-glass displays

The pinning of the OM6208 has an optimal design for single plane wiring, e.g. for chip-on-glass display modules.

16.3 Application examples

In the following application examples, the required values of the external capacitors are:

- C_{VLCD} = 1 µF minimum
- C_{VDD}, C_{VDD1} and C_{VDD2} = 1 µF minimum
- Higher capacitor values can be used for the supply.

When the internal charge pump is used, the V_{LCD} lines must be short-circuited externally to ensure that the resistance between pads is zero. This is to allow the bias system to work correctly when BS[2:0] is not 000.

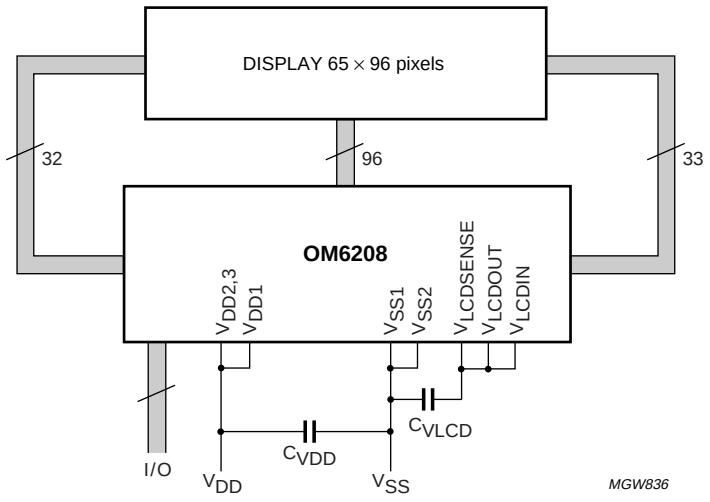


Fig.38 Application example using the internal charge pump and a single V_{DD} source.

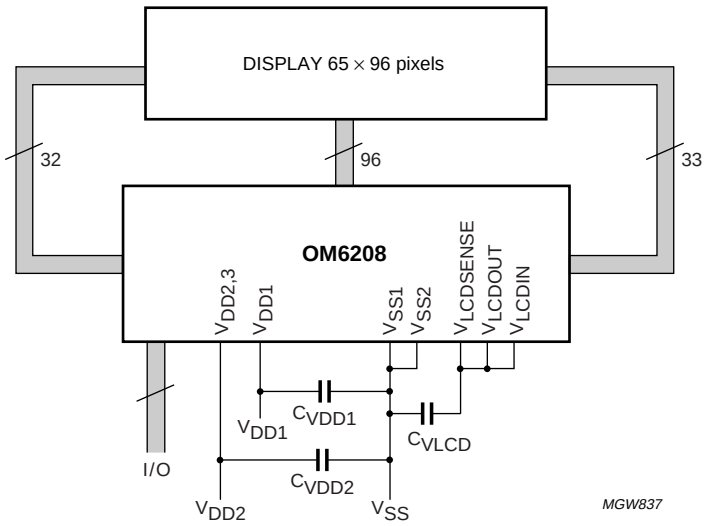


Fig.39 Application example using the internal charge pump and two separate V_{DD} sources (V_{DD1} and V_{DD2}).

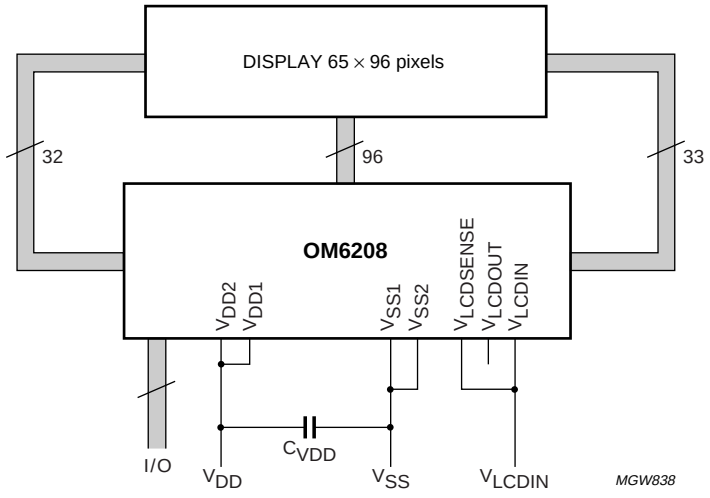


Fig.40 Application example using external high voltage generation.

17 MODULE MAKER PROGRAMMING

One Time Programmable (OTP) technology has been implemented in the OM6208. This enables the module maker to program some extended features of the OM6208 after it has been assembled on an LCD module. Programming is made under the control of the interfaces and the use of one special pin. This pin must be made available on the module glass but does not need to be accessed by the set maker.

The OM6208 features the following module maker programmable parameters:

- V_{LCD} calibration
- Default temperature compensation slopes
- Default charge pump multiplication factor
- Default V_{PR} value
- Default bias levels BS[2:0]
- Default frame frequency range in grey-scale mode GFR[2:0]
- Default oscillator tuning in grey-scale mode GT[2:0]
- Default frame frequency in black-and-white mode SFR[2:0]
- Default oscillator tune in black-and-white mode ST[2:0]
- Default N-line inversion NL[6:0]
- Default frame inversion FI
- Enable factory default FD
- Seal bit.

17.1 V_{LCD} calibration

The first OTP feature included is the ability to tune the V_{LCD} voltage with a 6-bit code (MMVOPCAL). This code is implemented in twos complement notation giving rise to a positive or negative offset to the V_{PR} register. The adder in the circuit has underflow and overflow protection. In the event of an overflow, the output will be clamped to 255; with an underflow, the output will be clamped to logic 0.

The final control to the high voltage generator, V_{OP}, will be the sum of all the calibration registers according to Section 11.10, equation (4).

Table 20 V_{LCD} calibration

MMVOPCAL						DECIMAL EQUIVALENT	V_{LCD} OFFSET (mV)
5	**4**	**3**	**2**	**1**	**0**		
0	1	1	1	1	1	31	930
0	1	1	1	1	0	30	900
0	1	1	1	0	1	29	870
:	:	:	:	:	:	:	:
0	0	0	0	1	0	2	60
0	0	0	0	0	1	1	30
0	0	0	0	0	0	0	0
1	1	1	1	1	1	–1	–30
1	1	1	1	1	0	–2	–60
:	:	:	:	:	:	:	:
1	0	0	0	1	0	–30	–900
1	0	0	0	0	1	–31	–930
1	0	0	0	0	0	–32	–960

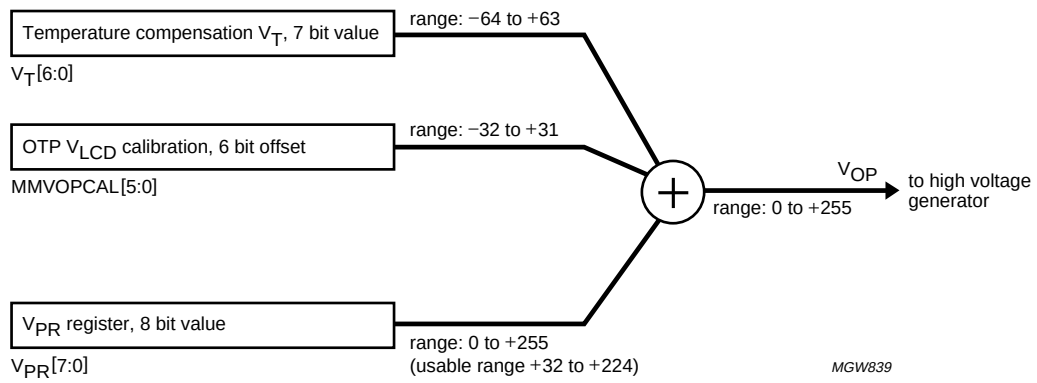


Fig.41 V_{LCD} calibration.

17.2 Factory defaults

17.2.1 Configuration derived from OTP cells

In some instances it is desirable that the configuration is derived from OTP cells and not from user-configurable registers. It is therefore possible to pre-define the following features using the OTP facility:

- Default temperature compensation slopes
- Default charge pump multiplication factor
- Default V_{PR} value
- Default bias levels BS[2:0]
- Default frame frequency range in grey-scale mode GFR[2:0]
- Default oscillator tune in grey-scale mode GT[2:0]
- Default frame frequency in black-and-white mode SFR[2:0]
- Default oscillator tune in black-and-white mode ST[2:0]
- Default N-line inversion NL[6:0]
- Default frame inversion FI
- Enable factory default FD
- Seal bit.

The selection of the mode for factory defaults is made by setting the factory default OTP cell bit MMFD.

Table 21 Factory default bit MMFD

MMFD	ACTION
0	configuration data is taken from the interface
1	OTP values are used for configuration data

The operation can be shown as a switch that selects between two sources of data (see Fig.42). When the OTP defaults are selected, changing the default values via the interface is not possible.

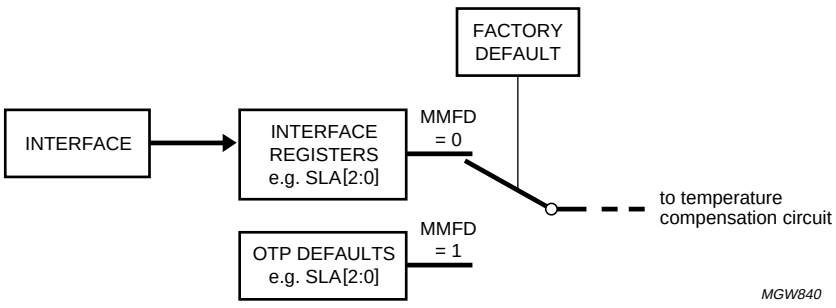


Fig.42 Factory defaults.

17.2.2 DEFAULTS FROM INTERFACE REGISTERS

Factory defaults available from user-configurable registers are as follows:

- Temperature slope selection values are set by SLA[2:0], SLB[2:0], SLC[2:0] and SLD[2:0]
- Default charge pump multiplication factor value is set by S[1:0]
- Default V_{PR} value is set by V_{PR}[7:0]
- Default bias level values are set by BS[2:0]
- Grey-scale mode default frame frequency and tuning values are set by GFR[2:0] and GT[2:0]
- Black-and-white mode default frame frequency and tuning values are set by SFR[2:0] and ST[2:0].

17.3 Seal bit

The module maker programming is performed in a special mode: the calibration mode (CALMM). This mode is entered via a special interface command, CALMM. To prevent wrongful programming, a seal bit has been implemented which prevents the device from entering the calibration mode. This seal bit, once programmed, cannot be reversed, thus further changes in programmed values are not possible. Applying the programming voltages when not in CALMM mode has no effect on the programmed values.

Table 22 Seal bit definition

SEAL BIT	ACTION
0	possible to enter calibration mode
1	calibration mode disabled

17.4 OTP architecture

The OTP circuitry in the OM6208 contains many bits of data. The circuitry for one bit is called an OTP slice. Each OTP slice consists of two main parts: the OTP cell (a non-volatile memory cell) and the shift register cell (a flip-flop). The OTP cells are accessible only through their shift register cells: both reading from and writing to the OTP cells are performed with the shift register cells, but only the shift register cells are visible to the rest of the circuit. The basic OTP architecture is shown in Fig.43.

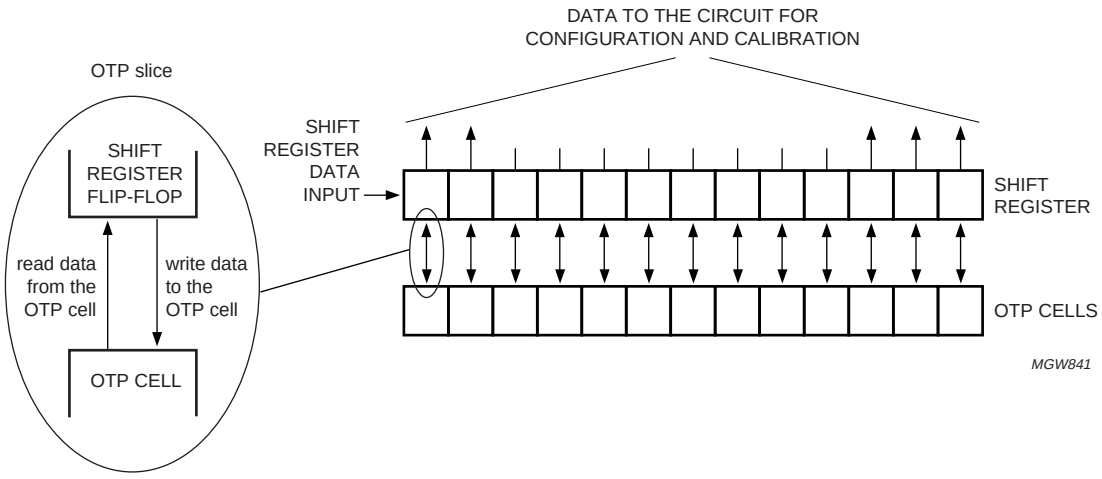


Fig.43 Basic OTP architecture.

17.4.1 OTP OPERATIONAL EFFECTS

The OTP architecture allows the following operations:

- Reading data from the OTP cells. The content of the non-volatile OTP cells is transferred to the shift register where upon it may affect the OM6208 operation.
- Writing data to the OTP cells. First, all 9 bits of data are shifted into the shift register via the interface. Then the content of the shift register is transferred to the OTP cells (there are some limitations related to storing data in these cells, see Section 17.7).
- Checking calibration without writing to the OTP cells. Shifting data into the shift register allows the effects on the V_{LCD} voltage to be observed.

The reading of data from the OTP cells is initiated by writing to the DON register. The OTP cells will not be updated until the device leaves power down and the oscillator starts. The reading operation needs up to 5 ms to complete.

The shifting of the data into the shift register is performed in the special mode CALMM. In the OM6208, the CALMM mode is entered through the CALMM command. Once in the CALMM mode the data is shifted into the shift register via the interface at the rate of 1-bit per command. After transmitting the last bit and exiting the CALMM mode the serial interface is again in the normal mode and all other commands can be sent. Care should be taken that always all bits of data (or a multiple of all bits) are transferred before exiting the CALMM mode, otherwise the bits will be in the wrong positions.

In the shift register the value of the seal bit is, like the other bits, always zero at reset. To make sure the security feature works correctly, the CALMM command is disabled until a Power-down mode has been left. Once a refresh is completed, the seal bit value in the shift register is valid and permission to enter CALMM mode can thus be determined.

The bits are shifted into the shift register in a predefined order as shown in Table 23.

Table 23 OTP bit order (See Fig.44 for a graphical representation)

POSITION	OTP CELL	POSITION	OTP CELL	POSITION	OTP CELL
1	MMVPR[7]	19	MMSLA[1]	37	MMGT[1]
2	MMVPR[6]	20	MMSLA[0]	38	MMGT[0]
3	MMVPR[5]	21	MMS[1]	39	MMSFR[2]
4	MMVPR[4]	22	MMS[0]	40	MMSFR[1]
5	MMVPR[3]	23	MMBS[2]	41	MMSFR[0]
6	MMVPR[2]	24	MMBS[1]	42	MMST[2]
7	MMVPR[1]	25	MMBS[0]	43	MMST[1]
8	MMVPR[0]	26	MMFD	44	MMST[0]
9	MMSLD[2]	27	MMVOPCAL[5]	45	MMNL[6]
10	MMSLD[1]	28	MMVOPCAL[4]	46	MMNL[5]
11	MMSLD[0]	29	MMVOPCAL[3]	47	MMNL[4]
12	MMSLC[2]	30	MMVOPCAL[2]	48	MMNL[3]
13	MMSLC[1]	31	MMVOPCAL[1]	49	MMNL[2]
14	MMSLC[0]	32	MMVOPCAL[0]	50	MMNL[1]
15	MMSLB[2]	33	MMGFR[2]	51	MMNL[0]
16	MMSLB[1]	34	MMGFR[1]	52	MMFI
17	MMSLB[0]	35	MMGFR[0]	53	SEAL
18	MMSLA[2]	36	MMGT[2]	–	–

17.5 Interface commands

Table 24 OTP instructions

These instructions are in addition to those in the Instruction set, Table 7.

NAME	D/$\overline{C}$	COMMAND BYTE								ACTION
		D7	D6	D5	D4	D3	D2	D1	D0	
OTP programming	0	1	1	1	1	0	0	OSE	CALMM	enter calibration mode and control programming
DON (refresh)	0	1	0	1	0	1	1	1	DON	display ON/OFF
Load 0	0	1	1	0	1	1	0	0	0	write 0 to shift register
Load 1	0	1	1	0	1	1	0	0	1	write 1 to shift register

17.5.1 CALMM INSTRUCTION

This instruction enters the device into the calibration mode. This mode enables the shift register for loading and allows programming of the non-volatile OTP cells to take place. If the seal bit is set, then this mode cannot be accessed and the instruction will be ignored. Once in calibration mode, data may be loaded into the shift register via the ‘LOAD0’ and ‘LOAD1’ instructions (on the falling edge of SCLK).

The CALMM mode may be left by setting the CALMM bit to logic 0. Reset will also clear this mode.

The programming can only take place when OTP Switch Enable (OSE) has been set to logic 1. This bit enables the $V_{OTPPROG}$ input to be passed to the OTP cells. This allows $V_{OTPGATE}$ to be tied to SCLH/$\overline{SCE}$ on the module for normal operation. Reset will also clear this mode.

17.5.2 REFRESH INSTRUCTION

The action of the ‘refresh’ instruction is to force the OTP shift register to reload from the non-volatile OTP cells. This instruction takes up to 5 ms to complete. During this time all other instructions may be sent.

In the OM6208 the ‘refresh’ instruction is associated with the ‘DON’ instruction so that the shift register is automatically refreshed every time DON is enabled or disabled.

Note: If this instruction is sent while in power save mode, the DON bit will be updated but the refreshing is delayed until the device leaves power-down.

17.6 Example of filling the shift register

An example sequence of commands and data is shown in Table 25. In this example the shift register is filled with the following data: MMVPR = 11010000, and the seal bit is logic 0.

It is assumed that the OM6208 has just been reset. After transmitting the last bit, the OM6208 can exit or remain in CALMM mode (see step 1). Note that while in CALMM mode the interface does not recognize commands in the normal sense.

After this sequence has been applied it is possible to observe the impact of the data shifted in. The sequence described is not useful for OTP programming because the number of bits with the value logic 1' is greater than that allowed for programming (see Section 17.7). The shift register contents after this action are shown in Fig.44.

Table 25 Example sequence for filling the shift register

STEP	D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	ACTION
1	0	1	0	1	0	1	1	1	1	exit power-down
2										wait 5 ms for refresh to take effect
3	0	1	1	1	1	0	0	0	1	enter CALMM mode
4	0	1	1	0	1	1	0	0	1	shift in data, first bit is MMVPR[7]; note 1
5	0	1	1	0	1	1	0	0	1	MMVPR[6]
6	0	1	1	0	1	1	0	0	0	MMVPR[5]
7	0	1	1	0	1	1	0	0	1	MMVPR[4]
8	0	1	1	0	1	1	0	0	0	MMVPR[3]
9	0	1	1	0	1	1	0	0	0	MMVPR[2]
10										
:	:	:	:	:	:	:	:	:	:	
57	0	1	1	0	1	1	0	0	1	MMFI
58	0	1	1	0	1	1	0	0	0	seal bit
59	0	1	1	1	1	0	0	0	0	exit CALMM mode

Note

1. The data for the bits is not in the correct shift register position until all bits have been sent.

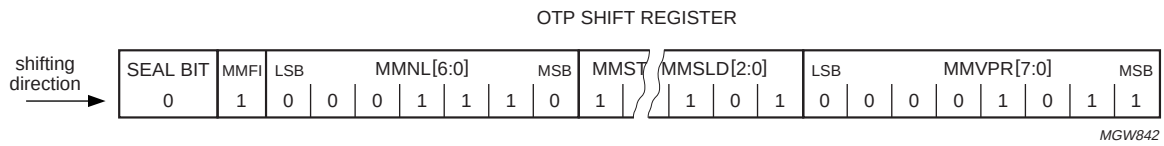


Fig.44 Shift register contents after example sequence of Table 25.

17.7 Programming flow

Programming is achieved whilst in CALMM mode and with the application of the programming voltages. As the data for programming the OTP cell is contained in the corresponding shift register cell, the shift register cell must be loaded with a logic 1 in order to program the corresponding OTP cell. If the shift register cell contains a logic 0, then no action will take place when the programming voltages are applied.

Once an OTP cell is programmed it cannot be de-programmed. An already programmed cell (an OTP cell containing a logic 1) must not be reprogrammed.

A sequence of commands and data for OTP programming is shown as an example in Table 26.

Although the order for programming cells is not significant, it is recommended that the seal bit is programmed last. Once this bit has been programmed it will not be possible to re-enter the CALMM mode.

During programming, a substantial current flows in the V_{LCDIN} pin. For this reason it is recommended programming only one OTP cell at a time. This is achieved by filling all but one shift register cells with logic 0.

The programming specification refers to the voltages at the chip pads, therefore the contact resistance is significant and must be considered by the user.

Table 26 Sequence for OTP programming

This sequence assumes the OM6208 has just been reset.

STEP	D/$\overline{C}$	D7	D6	D5	D4	D3	D2	D1	D0	ACTION
1	0	1	0	1	0	1	1	1	1	exit power-down (DON = 1)
2										wait 5 ms for refresh to take effect
3	0	1	1	1	1	0	0	1	1	enter CALMM mode and OSE
4	0	1	1	0	1	1	0	0	1	shift-in data, MMVPR[7] is first bit; note 1
5	0	1	1	0	1	1	0	0	0	MMVPR[6]
6	0	1	1	0	1	1	0	0	0	MMVPR[5]
7	0	1	1	0	1	1	0	0	0	MMVPR[4]
7	0	1	1	0	1	1	0	0	0	MMVPR[3]
9	0	1	1	0	1	1	0	0	0	MMVPR[2]
10										
:	:	:	:	:	:	:	:	:	:	
58	0	1	1	0	1	1	0	0	0	MMFI
59	0	1	1	0	1	1	0	1	0	seal bit
60										apply programming voltage at pins $V_{OTPPROG}$ and V_{LCDIN} according to Section 17.8
Repeat steps 5 to 60 for each bit that should be programmed to 1										
61										apply external reset

Note

1. The data for the bits is not in the correct shift register position until all the bits have been sent.

17.8 Programming specification

Table 27 Programming specification (refer to Fig.45)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
$V_{OTPPROG}$	voltage applied to pad $V_{OTPPROG}$	$V_{OTPPROG}$ relative to V_{SS1}; note 1				
		programming active	11.0	11.5	12.0	V
		programming inactive	V_{SS} − 0.2	0	V_{DD1}	V
V_{LCDIN}	voltage applied to pad V_{LCDIN}	V_{LCDIN} relative to V_{SS1}; notes 1 and 2				
		programming active	9.0	9.5	10.0	V
		programming inactive	V_{SS2}	V_{DD2}	4.5	V
I_{LCDIN}	current drawn by pad V_{LCDIN} during programming	when programming a single bit to logic 1	–	850	1000	µA
$I_{OTPPROG}$	current drawn by pad $V_{OTPPROG}$ during programming		–	100	200	µA
T_{PROG}	ambient temperature during programming		0	25	40	°C
$t_{su(SCLK)}$	internal data set-up time after last clock		1	–	–	µs
$t_{hd(SCLK)}$	internal data hold time before next clock		1	–	–	µs
$t_{su(gate)}$	$V_{OTPPROG}$ gate set-up time prior to programming		1	–	10	µs
$t_{hd(gate)}$	$V_{OTPPROG}$ gate hold time after programming		1	–	10	µs
t_{PW}	pulse width of programming voltage		100	120	200	ms

Notes

1. The voltage drop across the ITO track and zebra connector must be taken into account to guarantee sufficient voltage at the chip pads.
2. The Power-down mode (DON = 0 and DAL = 1) and CALMM mode must be active while the V_{LCDIN} input is being driven.

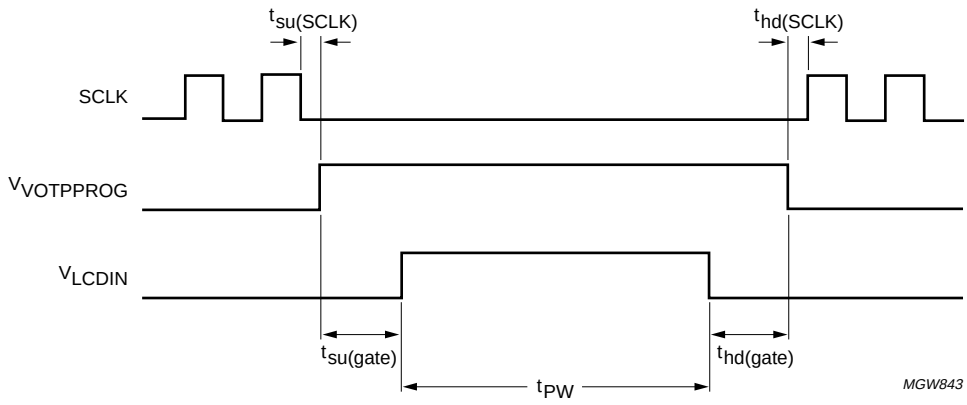
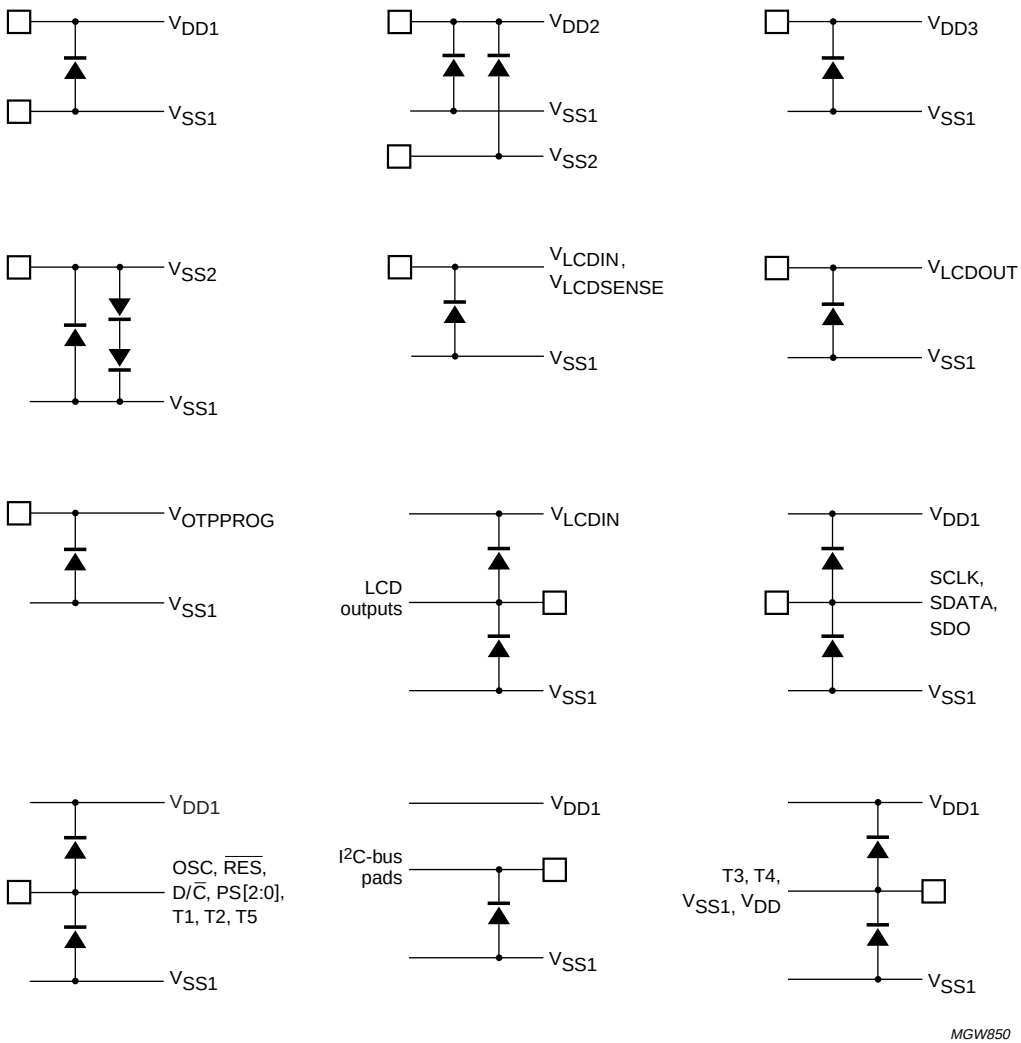


Fig.45 Programming waveforms.

18 DEVICE PROTECTION DIAGRAM



Protection diode maximum forward current = 5 mA.

Fig.46 Protection circuit diagrams.

19 BONDING PAD INFORMATION

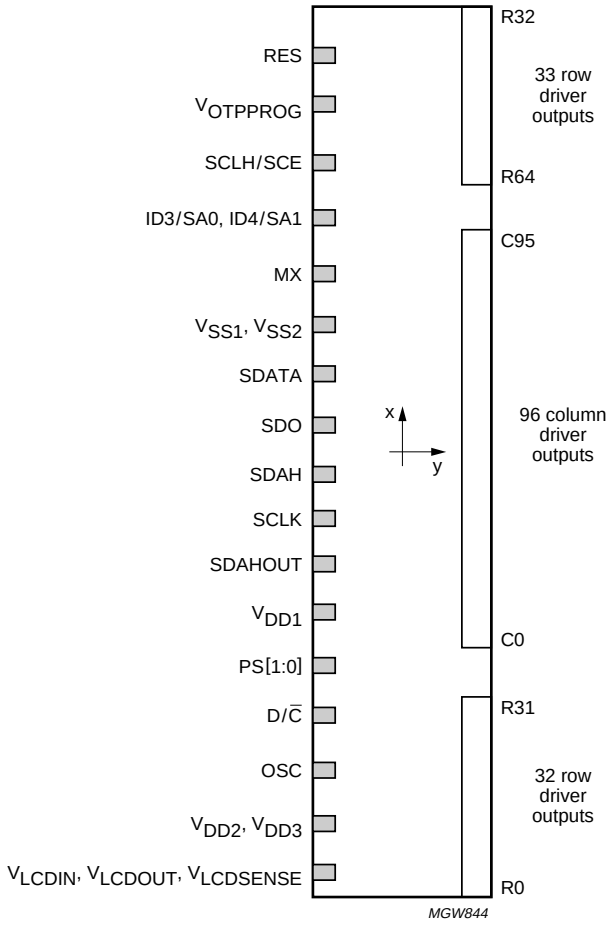


Fig.47 Bonding pad locations (viewed from bump side).

Table 28 Bonding pad locations
All x and y coordinates indicate pad centres and are referenced to the centre of the chip; dimensions in μm (see Fig.47).

SYMBOL	PAD	COORDINATES	
		x	y
dummy	1	–4919	+1279
dummy	2	–4856	+1279
alignment mark	3	–4762	+1220
dummy	4	–4649	+1279
V_{LCDIN}	5	–4586	+1279
V_{LCDIN}	6	–4523	+1279
V_{LCDIN}	7	–4460	+1279
V_{LCDIN}	8	–4397	+1279
V_{LCDOUT}	9	–4323	+1279
V_{LCDOUT}	10	–4260	+1279
V_{LCDOUT}	11	–4197	+1279
V_{LCDOUT}	12	–4134	+1279
V_{LCDOUT}	13	–4071	+1279
V_{LCDOUT}	14	–4008	+1279
V_{LCDOUT}	15	–3945	+1279
V_{LCDSEN}	16	–3882	+1279
V_{DD2}	17	–3566	+1279
V_{DD2}	18	–3503	+1279
V_{DD2}	19	–3440	+1279
V_{DD2}	20	–3377	+1279
V_{DD2}	21	–3314	+1279
V_{DD2}	22	–3251	+1279
V_{DD2}	23	–3188	+1279
V_{DD2}	24	–3125	+1279
V_{DD2}	25	–3062	+1279
V_{DD2}	26	–2999	+1279
V_{DD3}	27	–2928	+1279
V_{DD3}	28	–2865	+1279
V_{DD3}	29	–2802	+1279
OSC	30	–2639	+1279
DC	31	–2475	+1279
PS1	32	–2345	+1279
PS0	33	–2217	+1279
V_{DD1}	34	–2102	+1279
V_{DD1}	35	–2039	+1279
V_{DD1}	36	–1976	+1279
V_{DD1}	37	–1913	+1279
V_{DD1}	38	–1850	+1279
V_{DD1}	39	–1787	+1279
dummy	40	–1669	+1279
dummy	41	–1503	+1279
dummy	42	–1337	+1279
dummy	43	–1172	+1279
SDAHOUT	44	–1006	+1279
dummy	45	–829	+1279
SCLK	46	–657	+1279
dummy	47	–468	+1279
dummy	48	–303	+1279
dummy	49	–137	+1279
dummy	50	29	1279
dummy	51	194	1279
SDAH	52	360	1279
SDO	53	605	1279
SDATA	54	696	1279
V_{SS2}	55	795	1279
V_{SS2}	56	858	1279
V_{SS2}	57	921	1279
V_{SS2}	58	984	1279
V_{SS2}	59	1047	1279
V_{SS2}	60	1110	1279
V_{SS2}	61	1173	1279
V_{SS1}	62	1246	1279
V_{SS1}	63	1309	1279
V_{SS1}	64	1372	1279
V_{SS1}	65	1435	1279
V_{SS1}	66	1498	1279
V_{SS1}	67	1561	1279
MX	68	1693	1279
T3	69	1865	1279
T4	70	2028	1279
T1	71	2114	1279
T2	72	2232	1279
T5	73	2350	1279
T6	74	2468	1279
ID3_SA0	75	2586	1279

SYMBOL	PAD	COORDINATES	
		x	y
ID4_SA1	76	2704	1279
VDD1	77	2849	1279
dummy	78	3005	1279
dummy	79	3171	1279
dummy	80	3336	1279
dummy	81	3502	1279
dummy	82	3667	1279
SCLH	83	3833	1279
$V_{OTPPROG}$	84	3958	1279
$V_{OTPPROG}$	85	4021	1279
$V_{OTPPROG}$	86	4084	1279
dummy	87	4243	1279
RES	88	4387	1279
dummy	89	4489	1279
dummy	90	4552	1279
dummy	91	4615	1279
dummy	92	4678	1279
alignment mark	93	4799	1220
bumps alignment mark	94	4902	1258
dummy	95	+4900	–1275
dummy	96	+4849	–1275
dummy	97	+4797	–1275
dummy	98	+4745	–1275
dummy	99	+4693	–1275
dummy	100	+4641	–1275
dummy	101	+4589	–1275
dummy	102	+4538	–1275
dummy	103	+4486	–1275
dummy	104	+4434	–1275
R32	105	+4330	–1275
R33	106	+4278	–1275
R34	107	+4227	–1275
R35	108	+4175	–1275
R36	109	+4123	–1275
R37	110	+4071	–1275
R38	111	+4019	–1275
R39	112	+3967	–1275
R40	113	+3916	–1275
R41	114	+3864	–1275

SYMBOL	PAD	COORDINATES	
		x	y
R42	115	+3812	–1275
R43	116	+3760	–1275
R44	117	+3708	–1275
R45	118	+3656	–1275
R46	119	+3604	–1275
R47	120	+3553	–1275
R48	121	+3501	–1275
R49	122	+3449	–1275
R50	123	+3397	–1275
R51	124	+3345	–1275
R52	125	+3293	–1275
R53	126	+3242	–1275
R54	127	+3190	–1275
R55	128	+3138	–1275
R56	129	+3086	–1275
R57	130	+3034.	–1275
R58	131	+2982	–1275
R59	132	+2931	–1275
R60	133	+2879	–1275
R61	134	+2829	–1275
R62	135	+2775	–1275
R63	136	+2723	–1275
R64	137	+2671	–1275
VC	138	+2620	–1275
dummy	139	+2568	–1275
dummy	140	+2516	–1275
T8	141	+2413	–1275
T7	142	+2360	–1275
V1_L	143	+2308	–1275
C95	144	+2257	–1275
C94	145	+2205	–1275
C93	146	+2153	–1275
C92	147	+2101	–1275
C91	148	+2049	–1275
C90	149	+1997	–1275
C89	150	+1946	–1275
C88	151	+1894	–1275
C87	152	+1842	–1275
C86	153	+1790	–1275

SYMBOL	PAD	COORDINATES	
		x	y
C85	154	+1738	–1275
C84	155	+1686	–1275
C83	156	+1635	–1275
C82	157	+1583	–1275
C81	158	+1531	–1275
C80	159	+1479	–1275
C79	160	+1427	–1275
C78	161	+1375	–1275
C77	162	+1324	–1275
C76	163	+1272	–1275
C75	164	+1219.86	–1275
C74	165	+1168	–1275
C73	166	+1116	–1275
C72	167	+1064	–1275
C71	168	+961	–1275
C70	169	+909	–1275
C69	170	+857	–1275
C68	171	+805	–1275
C67	172	+753	–1275
C66	173	+701	–1275
C65	174	+650	–1275
C64	175	+598	–1275
C63	176	+546	–1275
C62	177	+494	–1275
C61	178	+442	–1275
C60	179	+390	–1275
C59	180	+339	–1275
C58	181	+287	–1275
C57	182	+235	–1275
C56	183	+183	–1275
C55	184	+131	–1275
C54	185	+79	–1275
C53	186	+28	–1275
C52	187	–24	–1275
C51	188	–76	–1275
C50	189	–128	–1275
C49	190	–180	–1275
C48	191	–232	–1275
dummy	192	–283	–1275

SYMBOL	PAD	COORDINATES	
		x	y
dummy	193	–335	–1275
C47	194	–387	–1275
C46	195	–439	–1275
C45	196	–491	–1275
C44	197	–543	–1275
C43	198	–595	–1275
C42	199	–646	–1275
C41	200	–698	–1275
C40	201	–750	–1275
C39	202	–802	–1275
C38	203	–854	–1275
C37	204	–906	–1275
C36	205	–957	–1275
C35	206	–1009	–1275
C34	207	–1061	–1275
C33	208	–1113	–1275
C32	209	–1165	–1275
C31	210	–1217	–1275
C30	211	–1268	–1275
C29	212	–1320	–1275
C28	213	–1372	–1275
C27	214	–1424	–1275
C26	215	–1476	–1275
C25	216	–1528	–1275
C24	217	–1579	–1275
C23	218	–1683	–1275
C22	219	–1735	–1275
C21	220	–1787	–1275
C20	221	–1839	–1275
C19	222	–1891	–1275
C18	223	–1942	–1275
C17	224	–1994	–1275
C16	225	–2046	–1275
C15	226	–2098	–1275
C14	227	–2150	–1275
C13	228	–2202	–1275
C12	229	–2253	–1275
C11	230	–2305	–1275
C10	231	–2357	–1275

SYMBOL	PAD	COORDINATES	
		x	y
C9	232	–2409	–1275
C8	233	–2461	–1275
C7	234	–2513	–1275
C6	235	–2564	–1275
C5	236	–2616	–1275
C4	237	–2668	–1275
C3	238	–2720	–1275
C2	239	–2772	–1275
C1	240	–2824	–1275
C0	241	–2875	–1275
dummy	242	–2927	–1275
dummy	243	–2979	–1275
V1_H	244	–3031	–1275
V2_L	245	–3083	–1275
V2_H	246	–3135	–1275
R31	247	–3187	–1275
R30	248	–3238	–1275
R29	249	–3290	–1275
R28	250	–3342	–1275
R27	251	–3394	–1275
R26	252	–3446	–1275
R25	253	–3498	–1275
R24	254	–3549	–1275
R23	255	–3601	–1275
R22	256	–3653	–1275

SYMBOL	PAD	COORDINATES	
		x	y
R21	257	–3705	–1275
R20	258	–3757	–1275
R19	259	–3809	–1275
R18	260	–3860	–1275
R17	261	–3912	–1275
R16	262	–3964	–1275
R15	263	–4016	–1275
R14	264	–4068	–1275
R13	265	–4120	–1275
R12	266	–4171	–1275
R11	267	–4223	–1275
R10	268	–4275	–1275
R9	269	–4327	–1275
R8	270	–4379	–1275
R7	271	–4431	–1275
R6	272	–4483	–1275
R5	273	–4534	–1275
R4	274	–4586	–1275
R3	275	–4638	–1275
R2	276	–4690	–1275
R1	277	–4742	–1275
R0	278	–4794	–1275
dummy	279	–4845	–1275
dummy	280	–4897	–1275

Table 29 Chip information

ITEM	ROW/COL SIDE	UNIT
Row/column side		
Pad pitch	51.84 (minimum)	µm
CBB opening	15.3 × 5.4	µm
Bump dimensions	30.0 × 99 (±3)	µm
Bump height	15.0	µm
Minimum bump distance	21.8	µm
Wafer thickness (excl. bumps)	381 (±25)	µm
Interface side		
Pad pitch	63 (minimum)	µm
CBB opening	25.7 × 5.4	µm
Bump dimensions	42 × 90 (±3)	µm
Bump height	15.0	µm
Minimum bump distance	shortened bumps: 21 normal bumps: 22	µm
Wafer thickness (excl. bumps)	381 (±25)	µm

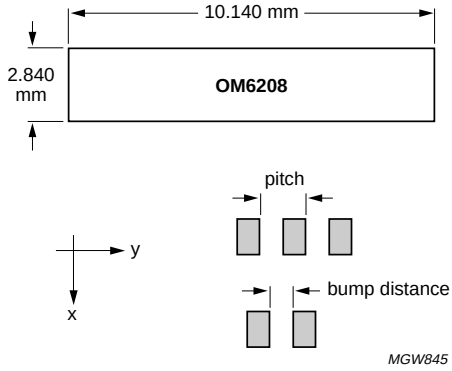


Fig.48 Chip size and pad pitch.

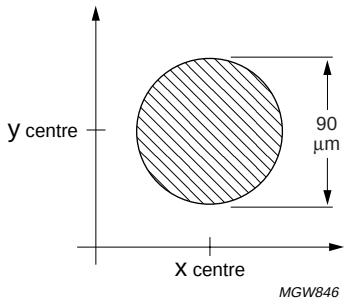


Fig.49 Shape of alignment mark.

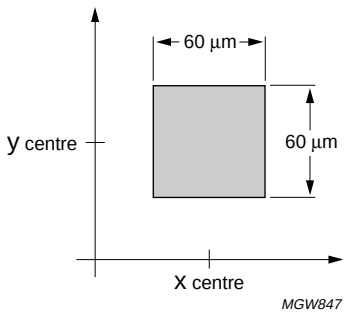


Fig.50 Shape of bump alignment mark.

20 TRAY INFORMATION

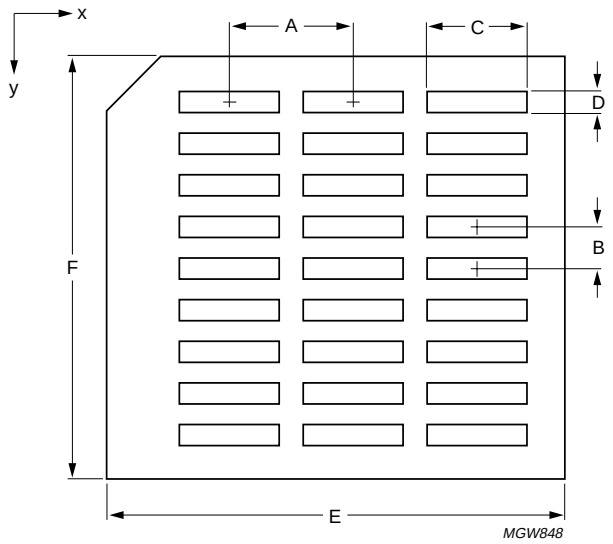
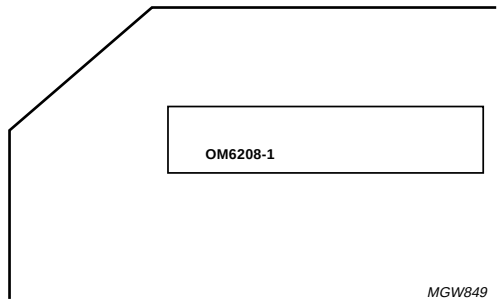


Fig.51 Tray details.



The orientation of the IC in a pocket is indicated by the position of the IC type name on the die surface with respect to the chamfer on the upper left corner of the tray. Refer to the bonding pad location diagram (Fig.47) for the orientation and position of the type name on the die surface.

Fig.52 Tray alignment.

Table 30 Tray dimensions

DIM.	DESCRIPTION	VALUE
A	pocket pitch, x direction	14.25 mm
B	pocket pitch, y direction	4.87 mm
C	pocket width, x direction	10.24 mm
D	pocket width, y direction	2.94mm
E	tray width, x direction	50.80 mm
F	tray width, y direction	50.80 mm
x	number of pockets in X direction	3
y	number of pockets in Y direction	9

21 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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